

# Selek MLK G5 AMD Schematics

## Renoir H

2019-12-16

REV : X02

*DY : None Installed*  
*UMA: UMA only installed*  
*PX: Discrete only*

Selek AMD



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A3

Document Number

**Selek MLK AMD**

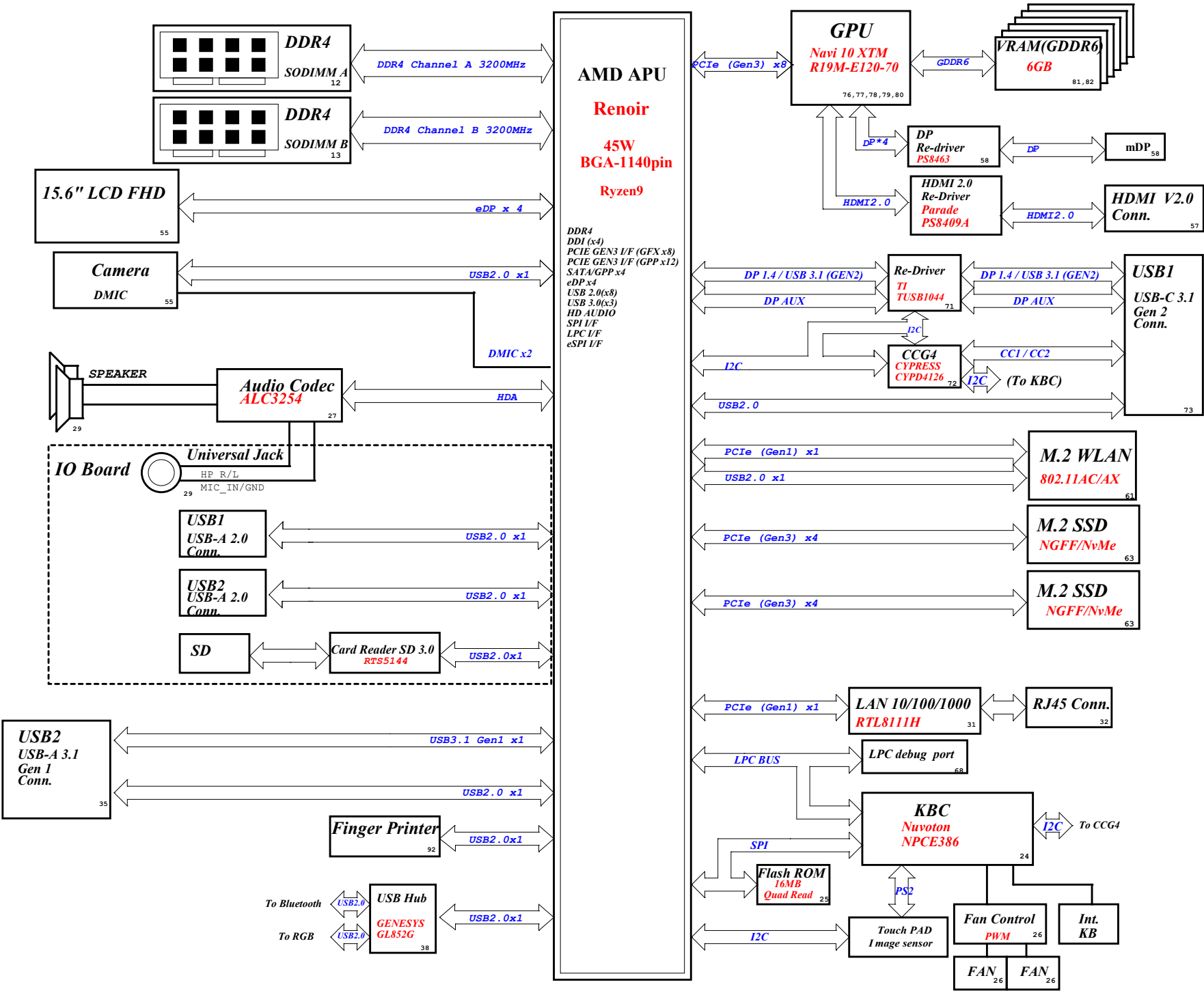
Rev

**A 00**

Date: Monday, December 16, 2019

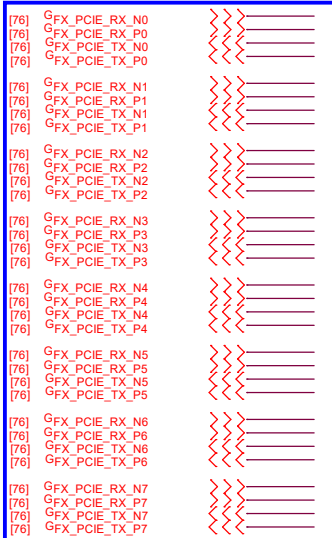
Sheet 1 of 106

MB	IO
19802	19A95
com	

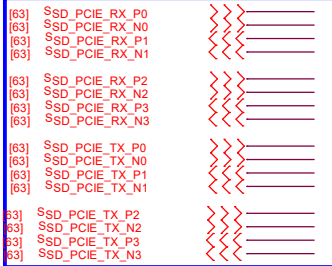


SSID = PCH

GPU



SSD1 M.2 (PCIE)



SSD2 M.2 (PCIE)



HDD

LAN



WLAN



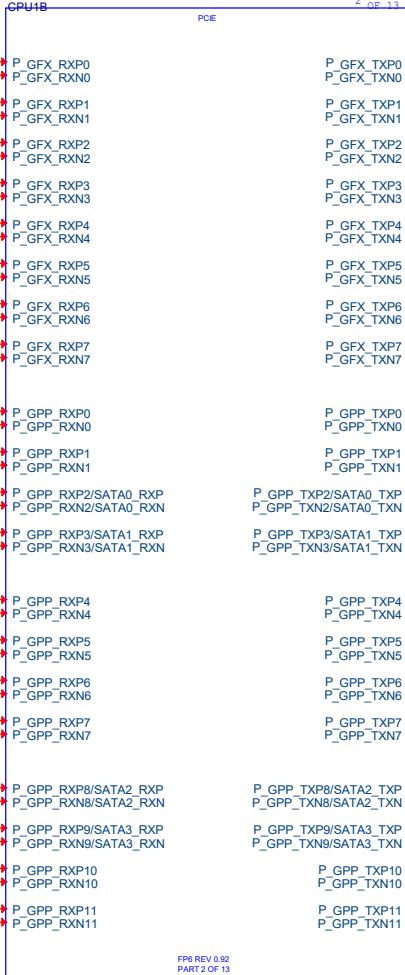
GPU

M.2 SSD1 (PCIE)

LAN  
WLAN

M.2 SSD2 (PCIE)

GPU & GPP, 85Ω



RENOIR-GP  
ZZ.00CPU.411

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Title: **CPU (PCIE/SATA)**

Size: A3 Document Number: **Selek MLK AMD** Rev: A00

Date: Monday, December 16, 2019 Sheet 3 of 106

5

4

3

2

1

D


C

B

A

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Selek AMD

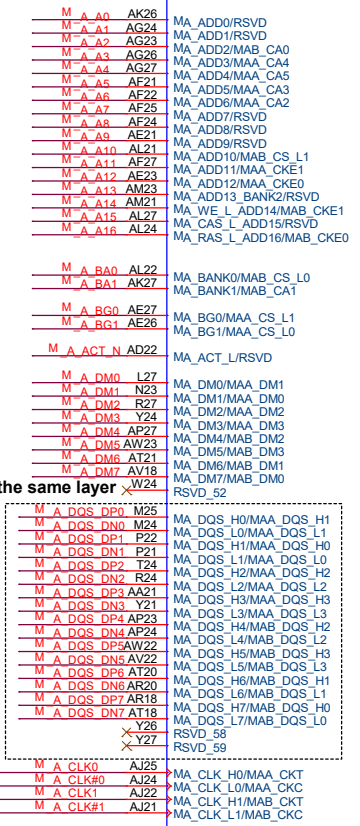
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (RSVD)			
Size	Document Number		Rev
A4	Selek MLK AMD		A00
Date:	Monday, December 16, 2019		Sheet 4 of 106

SSID = CPU



DDR4 Channel A to SO-DIMM

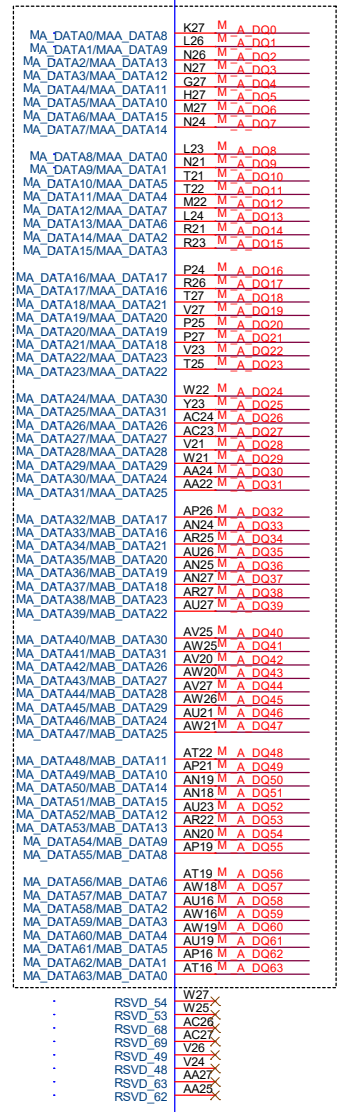
ADD and CLK on the sam layer



DM, DQ & DQS on the same layer

ADD, CMD, CTL, 40Q  
DATA CHECK, 50Q  
Misc. 40~60Q  
DDR CLK, 72Q  
DQS, 80Q

DM, DQ & DQS on the same layer



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Title: **CPU (DDR4 CHA)**

Size: A 3 Document Number: **Selek MLK AMD** Rev: **A 00**

Date: Monday, December 16, 2019 Sheet: 5 of 106

SSID = CPU

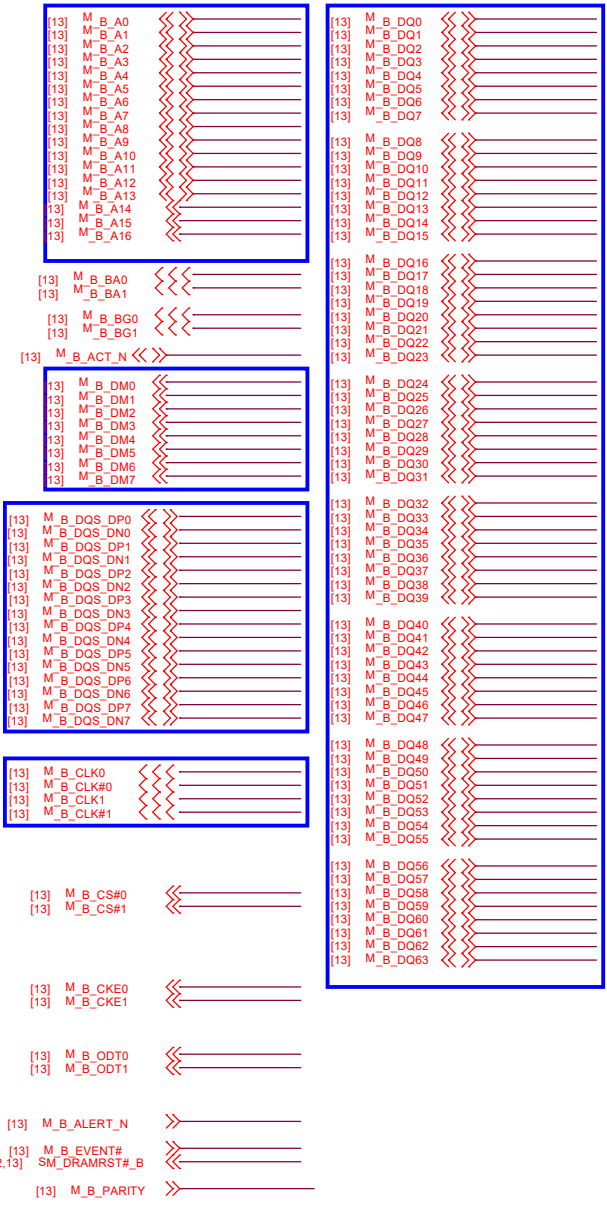
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ADD, CMD, CTL, 40Ω  
DATA CHECK, 50Ω  
Misc. 40~60Ω  
DDR CLK, 72Ω  
DQS, 80Ω

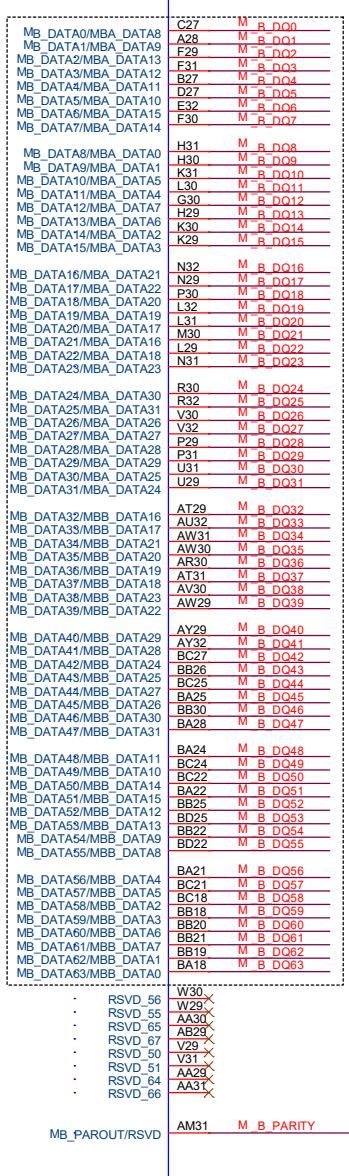
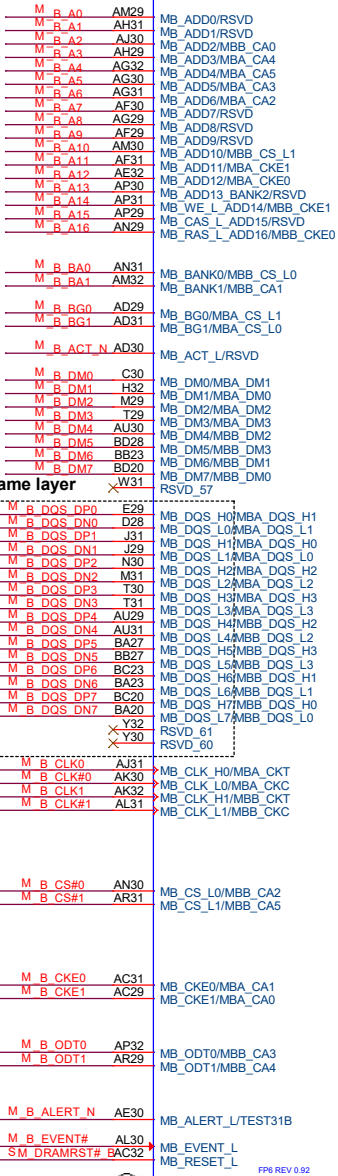
DDR4  
Channel B to SO-DIMM

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer



DM, DQ & DQS on the same layer



Signal GRP	Signal	Signal	Signal	Signal
Clocks	CLK			
Address	ADD	BANK	BG	
Command	RAS_L	CAS_L	WE_L	ACT
Control	CKE	ODT	CS_L	
Data	Data	DM	DQS	
Misc.	M_RESET_L	M_EVENT_L	M_ALERT	
M_PAROUT				



RENOIR-GP  
ZZ.00CPU.411

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Title

**CPU (DDR4 CHB)**

Size A 3

Document Number

**Selek MLK AMD**

Date: Monday, December 16, 2019

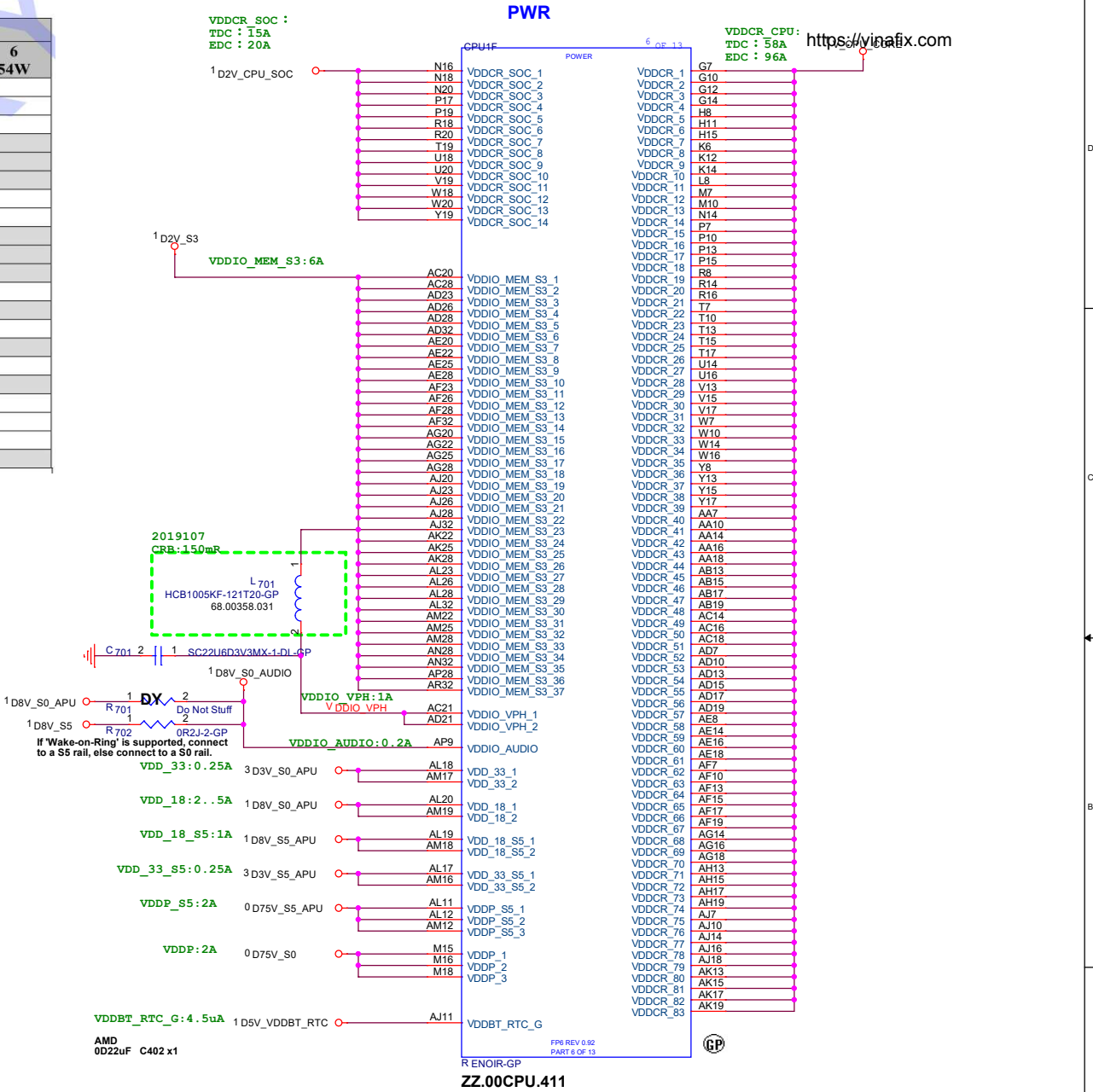
Rev

**A 00**

Sheet 6 of 106

Table 5. FP6 Processor Voltage Supply Currents

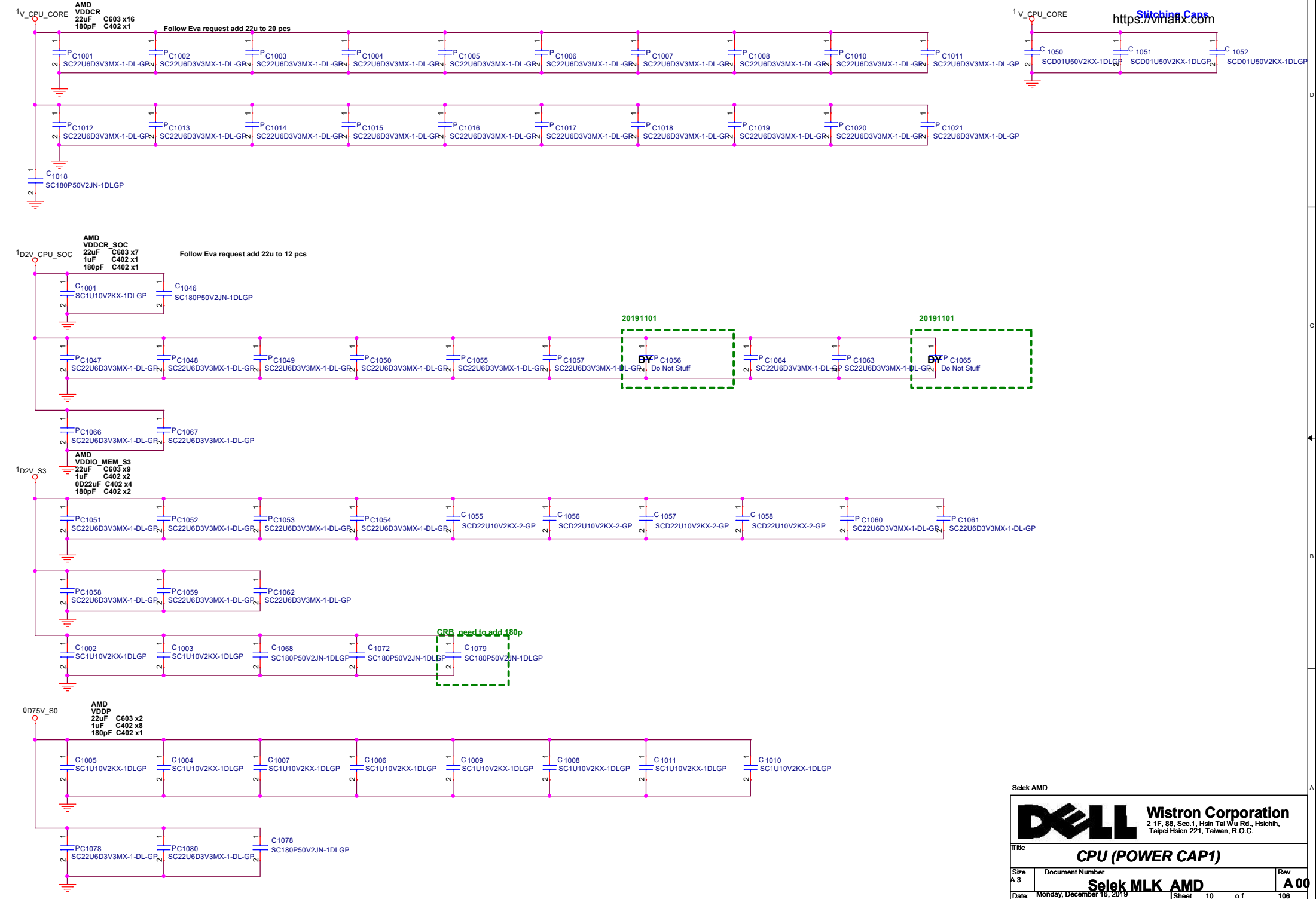
Supply <sup>1</sup>	Nominal Voltage at Pkg Ball (V) <sup>2</sup>	Condition	SYSTEM_CONFIGURATION					
			1 10W	2 15W	3 25W	4 35W	5 45W	6 54W
VDDCR_VDD	Variable (0.65–TBD) <sup>5</sup>	TDC <sup>3</sup>	20	33	44	51		58
		EDC	34	50	70	90		96
		Max Loadstep <sup>4</sup>	29	43	65	76		84
VDDCR_SOC	Variable (0.7–TBD) <sup>5</sup>	TDC <sup>3</sup>	10	13			15	
		EDC	13	17			20	
		Max Loadstep <sup>4</sup>						
VDDIO_MEM_S3 <sup>6</sup>	1.10	TDC				6.00		
		TDC				6.00		
		TDC				1.00		
VDDIO_VPH <sup>7</sup>	1.20	TDC				1.00		
		TDC				1.00		
		TDC				1.00		
VDDP	0.75	TDC				2.00		
VDDP_S5	0.75	TDC				2.00		
VDD_18	1.80	TDC				2.50		
VDD_18_S5	1.80	TDC				1.00		
VDD_33	3.30	TDC				0.25		
VDD_33_S5	3.30	TDC				0.25		
	1.20	TDC				0.20		
		TDC				0.20		
		TDC				0.20		
VDDIO_AUDIO	1.80	TDC				0.20		
VDDBT_RTC_G	3.00	TDC				4.5µA		

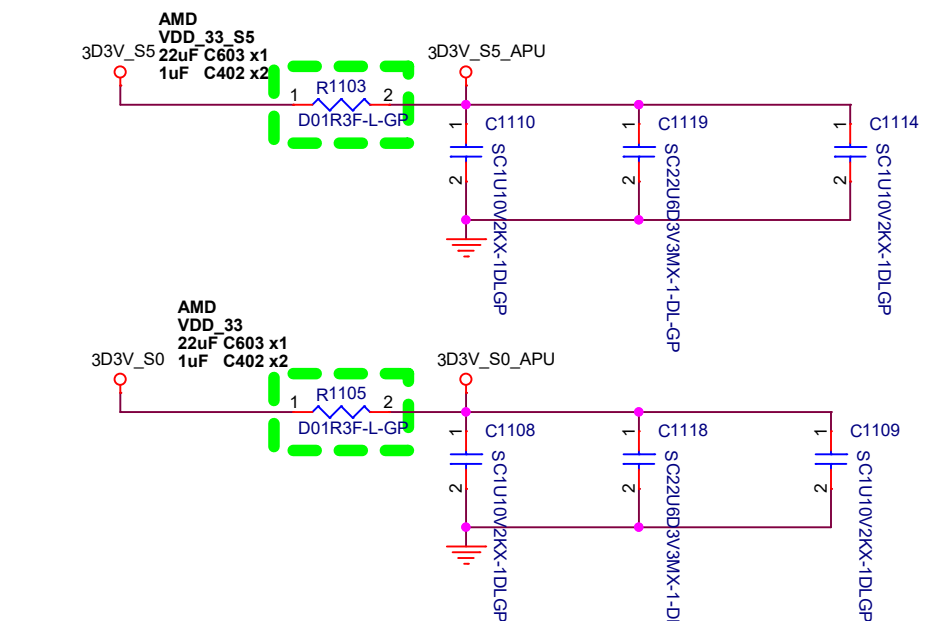
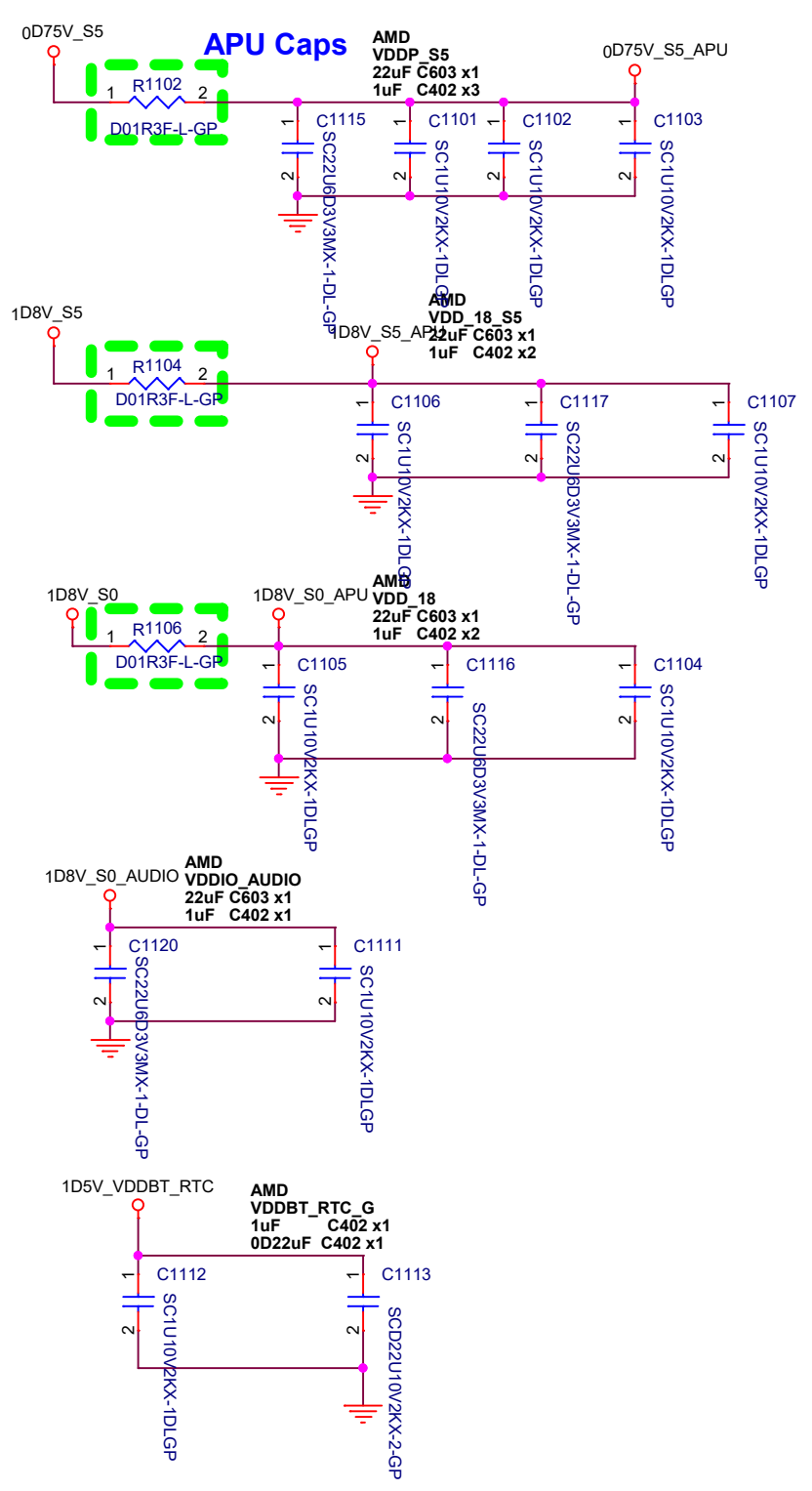






APU Caps






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Table 131. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_SOC	VDDIO_MEM_S3 <sup>1, 2</sup>	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTC_G
Value	Package Size / Material											
22 $\mu$ F	0603 X5R	15BU + 1BO	5BU + 2BO	7BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 $\mu$ F	0402 X5R	-	1BO	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BO	1BO
0.22 $\mu$ F	0402 X5R	-	-	4 along split	-	-	-	-	-	-	-	1BO
180 pF	0402 C0G NP0	1BU	1BO	1BU + 2 along split	1BU	-	-	-	-	-	-	-

Key: Capacitor locations are marked as follows: BU = Bottom, Under the processor, BO = Bottom, Outside of the processor, T = Top, same side as the Processor S = Close to VDDIO\_MEM\_S3 plane split

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Title

**CPU (POWER CAP2)**

Size A4

Document Number

Rev

**Selek MLK AMD**

**A00**

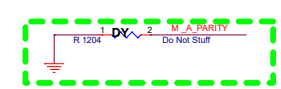
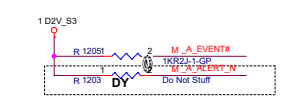
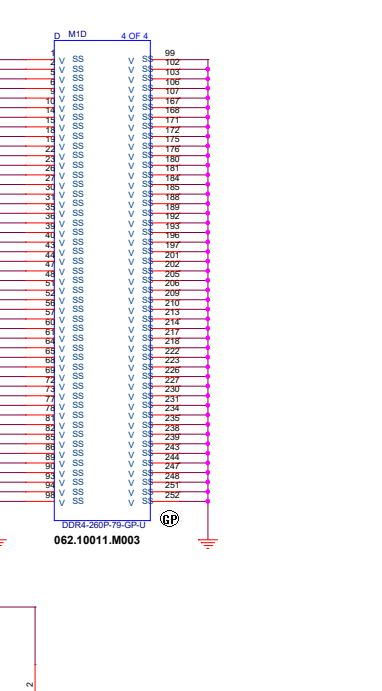
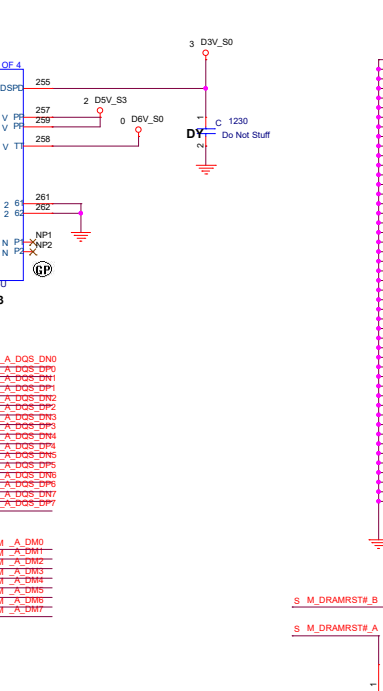
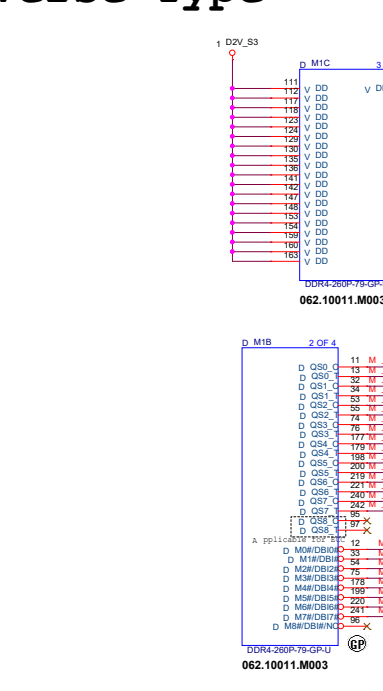
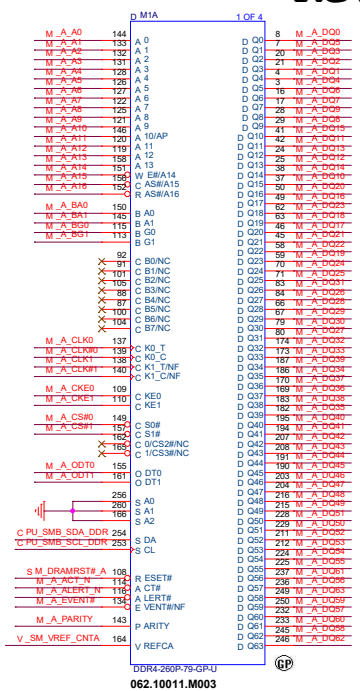
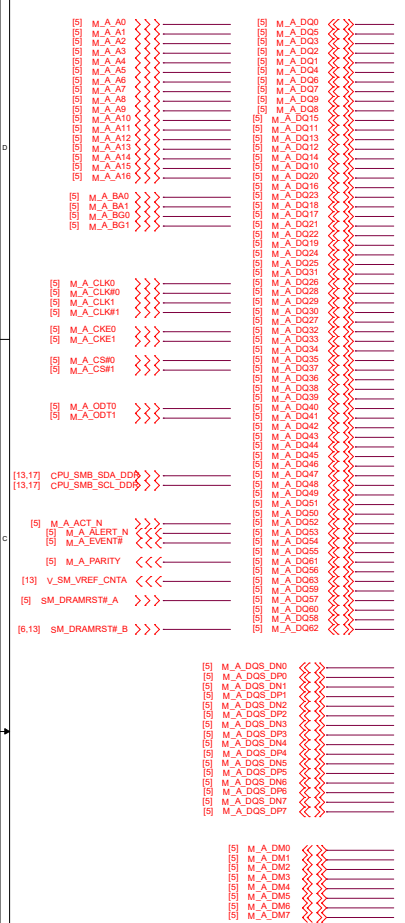
Date: Monday, December 16, 2019

Sheet 11 of 106

Main Func = DDR4 = SODIMM

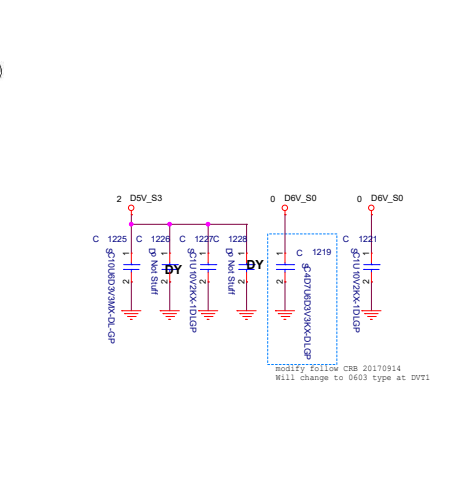
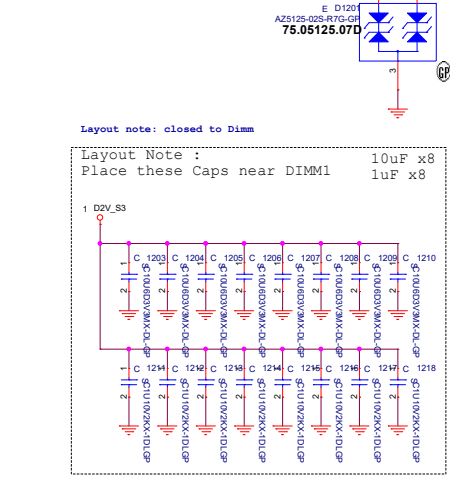
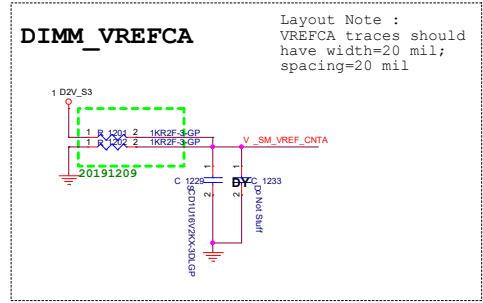
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Reverse Type

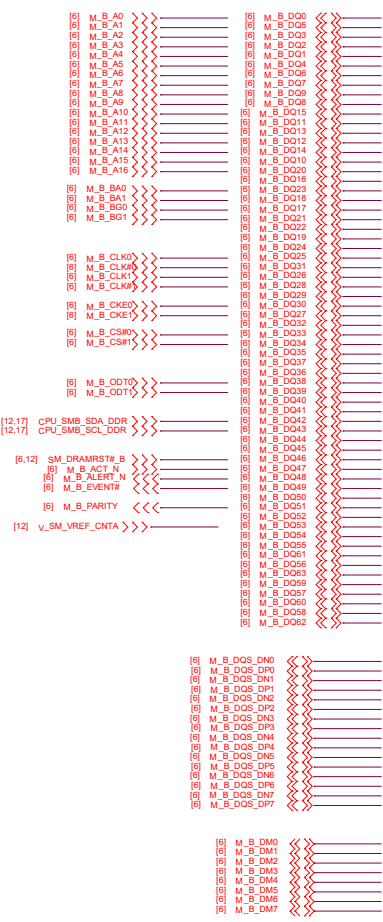


SPD Address of DIMM1

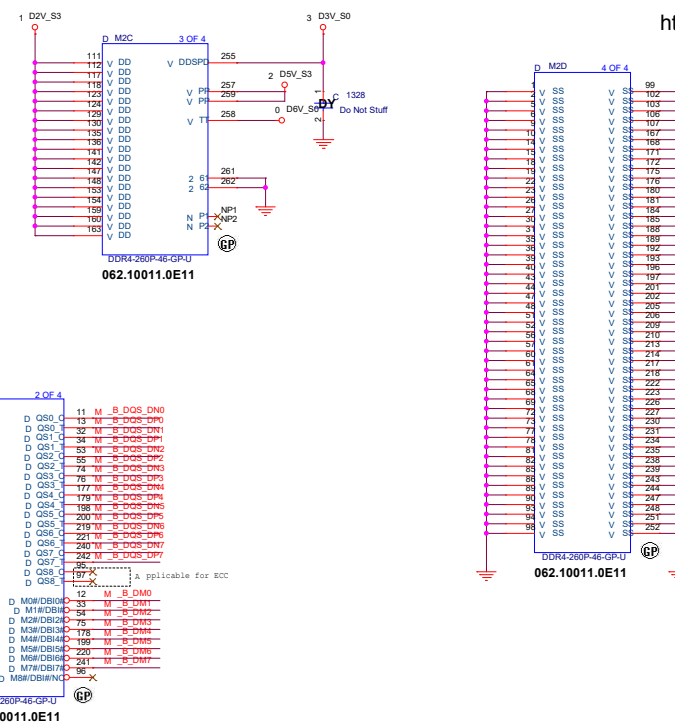
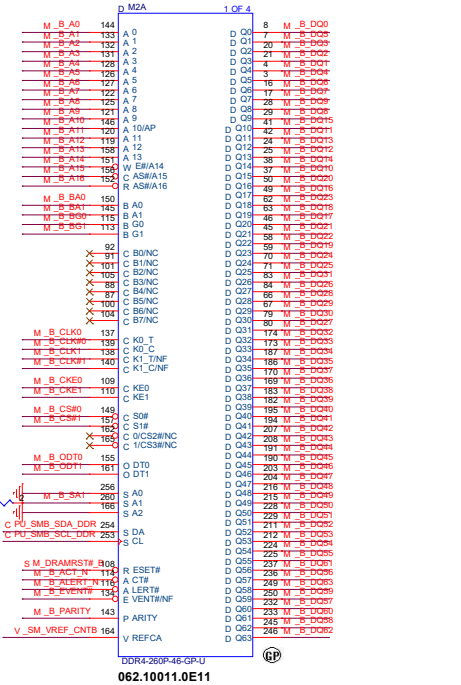
SPD SA2	0
SPD SA1	0
SPD SA0	0



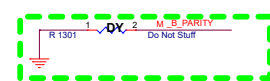
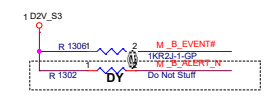
Main Func = DDR4 SODIMM



Reverse Type

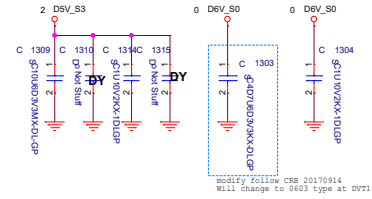
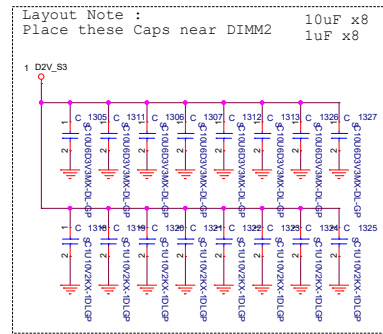
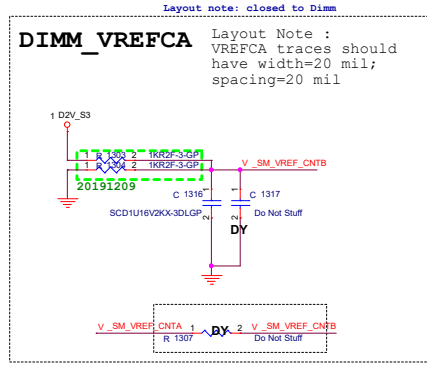


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SPD Address of DIMMB

SPD	SA2	0
SPD	SA1	1
SPD	SA0	0



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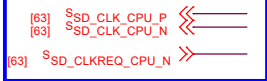
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>DDR (RSVD)</b>					
Size A4	Document Number <b>Selek MLK AMD</b>				Rev <b>A00</b>
Date: Monday, December 16, 2019			Sheet	14	of 106

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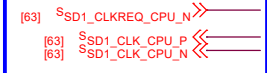
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>DDR (RSVD)</b>			
Size A4	Document Number <b>Selek MLK AMD</b>		Rev <b>A00</b>
Date: Monday, December 16, 2019		Sheet 15	of 106

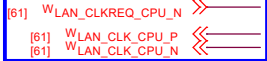
## SSD



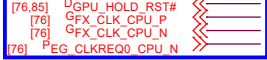
## SSD2



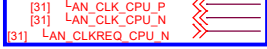
## WLAN



## DGPU



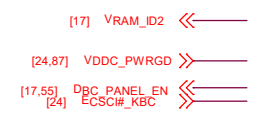
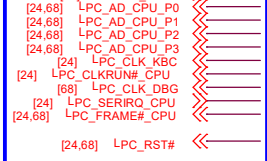
## LAN



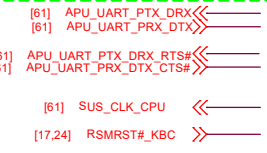
## SPI



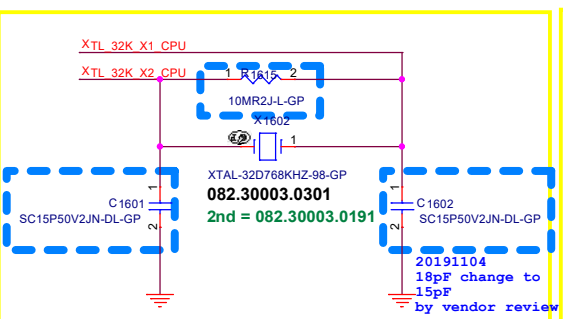
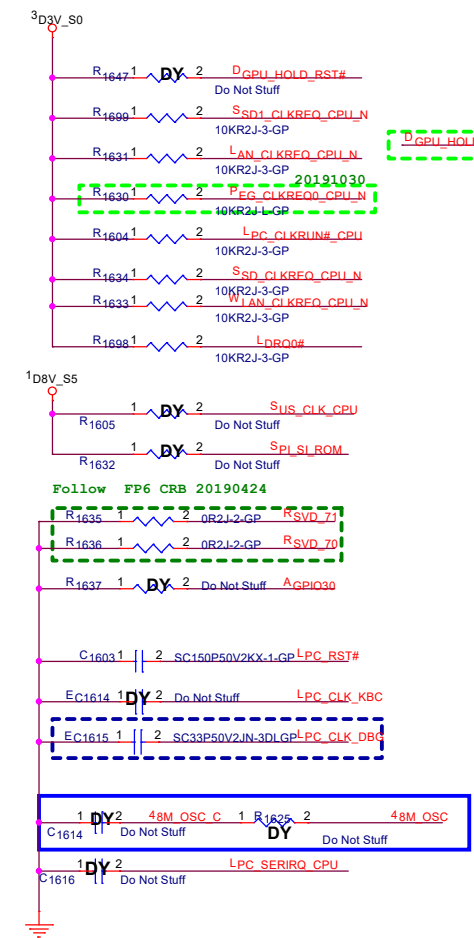
## LPC



## UART WLAN

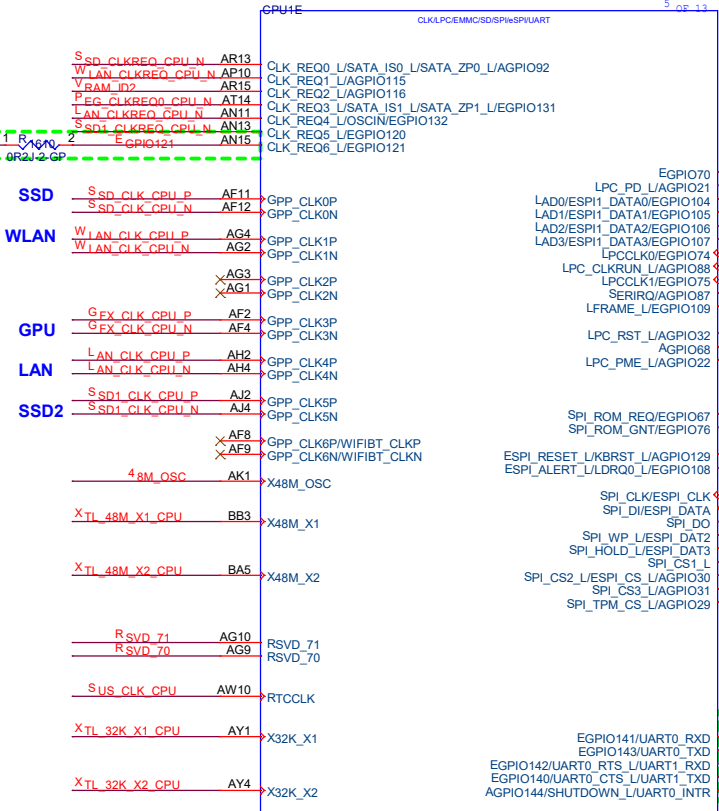


## CLK/SATA/USB/SPI/LPC

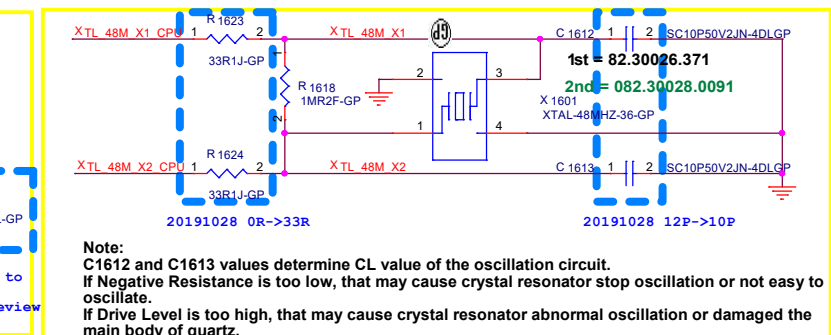


20191104  
18pF change to  
15pF  
by vendor review

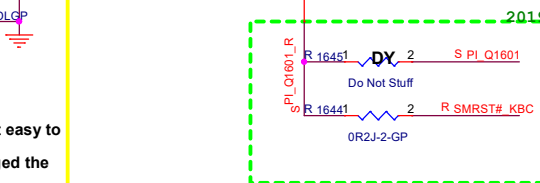
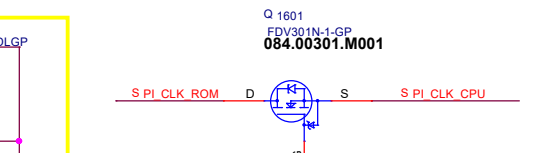
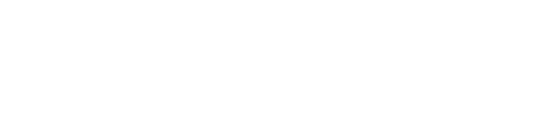
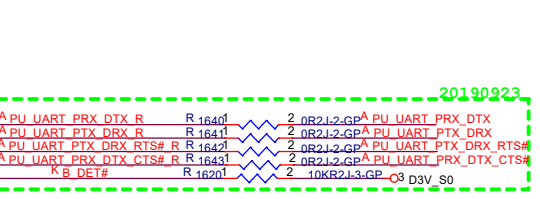
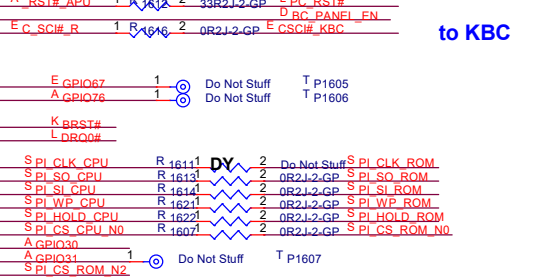
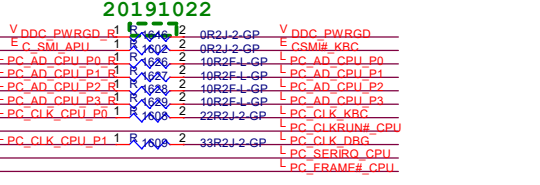
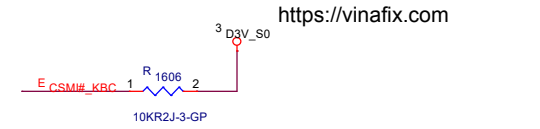
## GFX & GPP CLK, 850 SATA & USB, 900



ZZ.00CPU.411



Note:  
C1612 and C1613 values determine CL value of the oscillation circuit.  
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.  
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (CLK/LPC/SPI/UART)**

Size: A3 Document Number: **Selek MLK AMD** Rev: **A00**

Date: Monday, December 16, 2019 Sheet: 16 of 106

# SSID = PCH

## CLK/SATA/USB/SPI/LPC

### SO-DIMM

[12.13] CPU\_SMB\_SCL\_DDR <<<  
[12.13] CPU\_SMB\_SDA\_DDR <<<

### Touch Pad

[65.66] CPU\_I2C\_SCL\_P3 <<<  
[65.66] CPU\_I2C\_SDA\_P3 <<<

[27] HDA\_SDN0\_CPU >>>  
[27] HDA\_BITCLK\_CODECD\_R <<<  
[27] HDA\_SYNC\_CODECD <<<  
[27] HDA\_SDOOT\_CODECD <<<

[55] dMIC\_CLK\_EDP >>>  
[55] dMIC\_DATA\_EDP >>>

[24.44,51.65,92] APU\_SLP\_S3# <<<  
[24.40,51.52,57.58,65] APU\_SLP\_S3# <<<

[16.24] SPI\_01601 >>>

[24.61,63.68,76.91] PLT\_RST# >>>  
[24] PM\_PWRBTN# >>>  
[24.40] SYS\_PWRGD >>>  
[45.54] 3V\_SV\_PWRGD >>>

[20] SYS\_RST#\_CPU >>>  
[24.79] AC\_PRES\_KBC >>>

[24] PSP\_2 <<<  
[24] PSP\_1 <<<

[65] TP\_WAKE\_CPU# <<<  
[91] PIRQ# <<<

[64] SATA\_ACT# <<<

[27] SPKR <<<  
[65] KB\_LED\_BL\_DET >>>

[61] WLAN\_EN\_APU >>>

[63] PCIE\_SSD\_RST <<<  
[66.87] BOMACO\_EN <<<

[16.55] DBC\_PANEL\_EN <<<  
[16] VRAM\_ID2 >>>

[61] BLUETOOTH\_EN >>>  
[29] SKP\_ID >>>

[65] ELC\_Nrst <<<  
[65] BOOT0 <<<  
[65] ELC\_EN\_PCH <<<

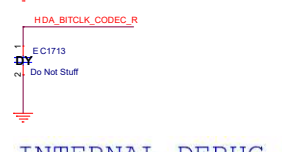
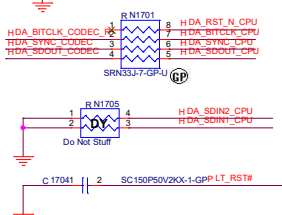
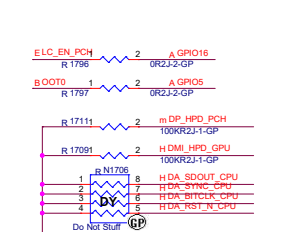
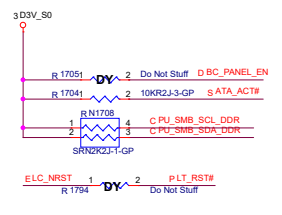
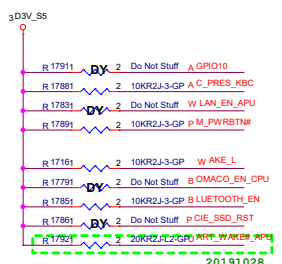
[57.79] HDMI\_HPD\_GPU <<<  
[58.79] mDP\_HPD\_PCH <<<

[61] DOUT\_BT\_M2 <<<  
[61] BCLK\_BT\_M2 >>>

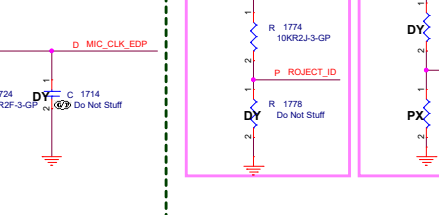
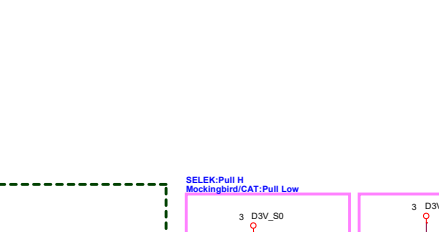
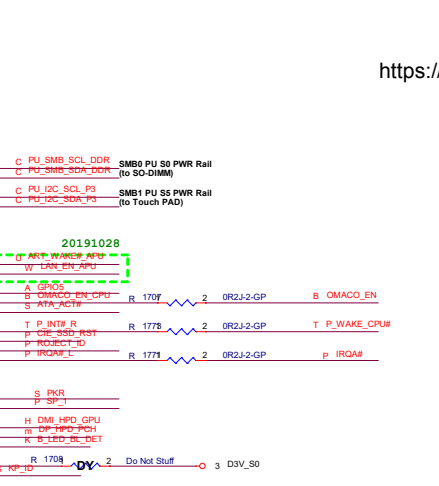
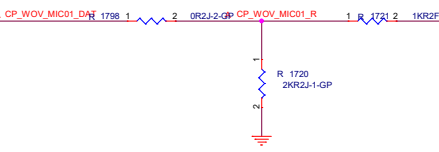
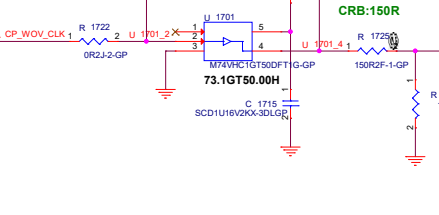
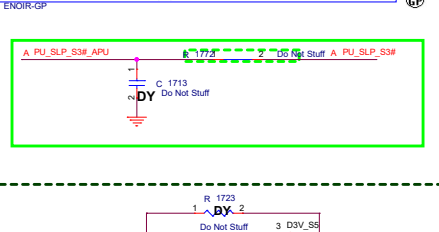
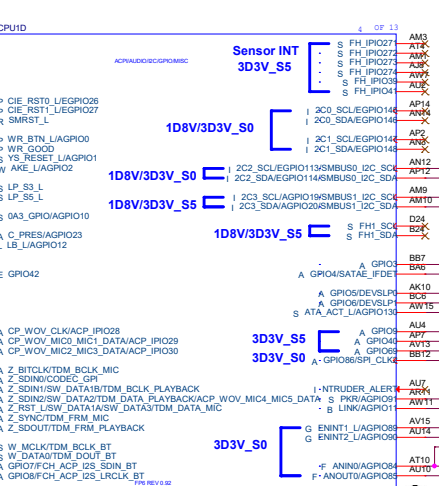
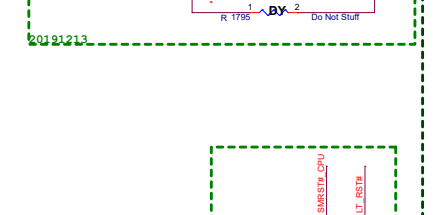
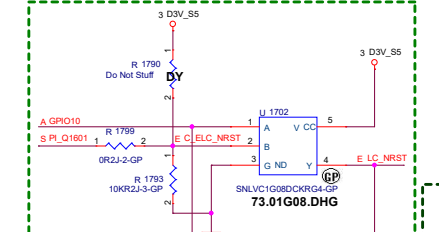
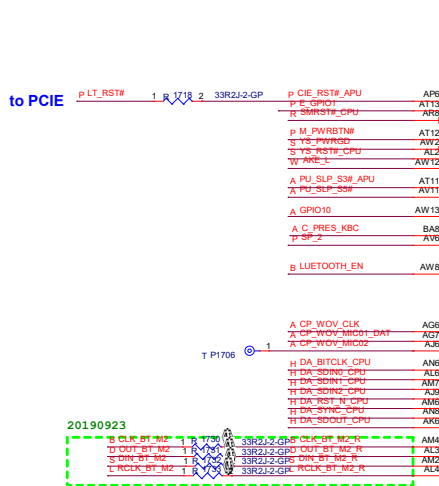
[61] LRCLK\_BT\_M2 >>>  
[61] SDIN\_BT\_M2 >>>

[76.86] PE\_GPIO1 <<<  
[61] UART\_WAKER\_APU >>>

[18] AGPIO16 >>>

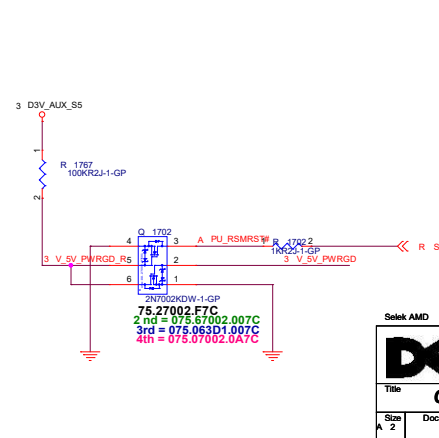
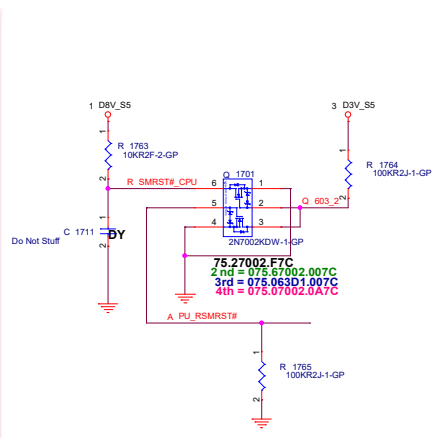
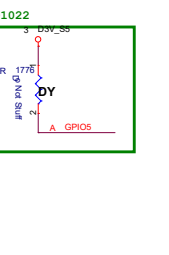
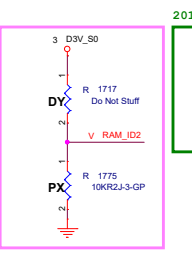
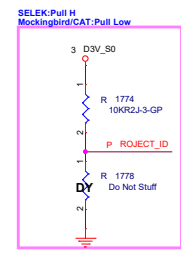


INTERNAL DEBUG PURPOSE ONLY			
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



Straps	LFRAME_L LPCLK6/EGPIO74 LPCLK6/EGPIO75 RTCLK SYS RESET_LIAGPIO1 BLINKUSB_DCT_LIAGPIO11 EGPIO3
S5 PWR Rail	AGPIO6 - EGPIO42
S0 PWR Rail	AGPIO64 - EGPIO148
SMB0, 3D3V_S0	DIMM
SMB1, 3D3V_S5	KBC 3D3V_S5 Thermal 3D3V_S0 GSENSOR for HDD Protect

https://vinafix.com



Selek AMD

Wistron Corporation  
2 - 1F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title	CPU (I2C/GPIO/RTC/SMBUS/HDA)
Size	2
Document Number	Selek MLK_AID
Date	Monday, December 16, 2019
Sheet	17
Rev	A 00

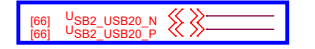
Main Func = USB

https://vinafix.com

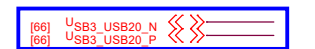
USB3.0 Port1



USB2.0 Port2



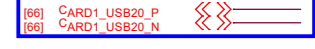
USB2.0 Port3



HUB USB20



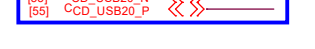
Card Reader



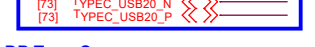
Finger Printer



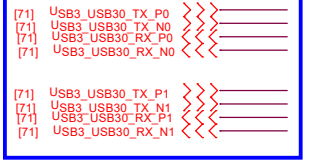
IR Camera



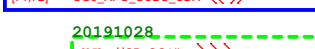
Type C USB20



DP Type-C



DP Type-C



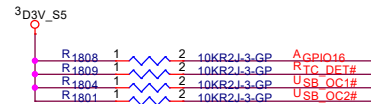
20191028



20191022



USB_OC0#	ELC_EN_PCH
USB_OC1#	USB3.0 Power
USB_OC2#	USB2.0 Power
USB_OC3#	RTC_DET#



Type-C

USB3.0 Port1

Card Reader

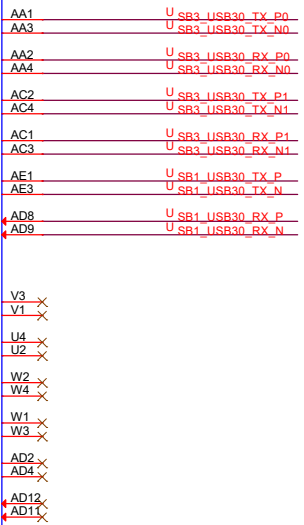
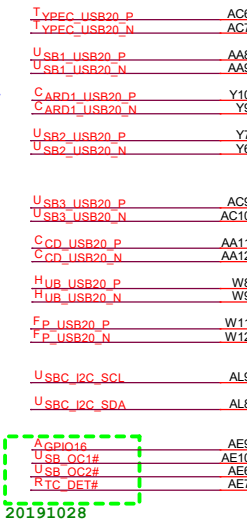
USB2.0 Port1

USB2.0 Port2

IR Camera

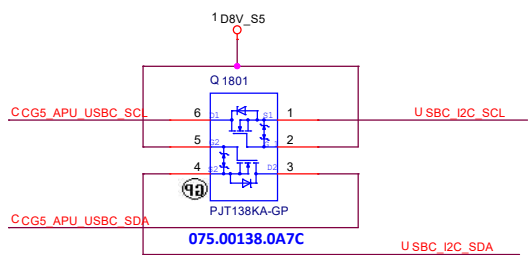
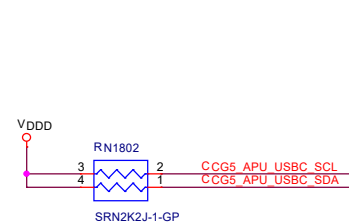
HUB USB20

Finger Printer



ZZ.00CPU.411

AGPIO13/USB\_OC5\_L  
If unused,  
enable internal pull up or pull down by software.



Selek AMD

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.


Title: **CPU (USB)**

Size: A3 Document Number: **Selek MLK\_AMD** Rev: **A00**

Date: Monday, December 16, 2019 Sheet: 18 of 106

(Blanking)

Selek AMD



**Wistron Corporation**  
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (RSVD)

Size  
A 3

Document Number  
**Selek MLK AMD**

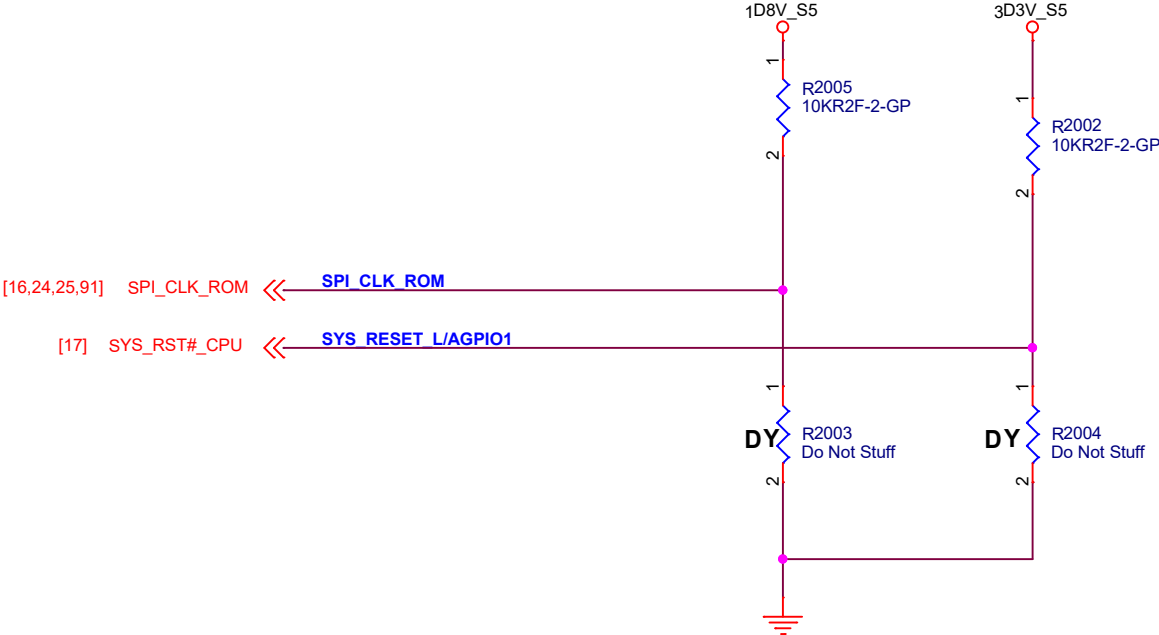
Date: Monday, December 16, 2019

Rev  
**A 00**

Sheet 19 of 106


STRAP PINS

https://vinafix.com



	PIN SPI_CLK NET SPI_CLK_ROM	PIN SYS_RESET_L//AGPIO1 NET SYS_RST#_CPU
PULL HIGH	Configured for internal clock-generator 10kΩ(± 5%) pull-up resistor to VDD_18 (DEFAULT)	Normal powerup / reset timing 10kΩ(± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)
PULL LOW	Reserved	Reserved

Selek AMD



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (Strap)**

Size  
A4

Document Number  
**Selek MLK AMD**


Rev  
**A00**

Date: Monday, December 16, 2019

Sheet 20 of 106

(Blanking)

Selek AMD



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (RSVD)

Size  
A 3

Document Number  
**Selek MLK AMD**


Date: Monday, December 16, 2019

Rev  
**A 00**

Sheet 21 of 106

(Blanking)

Selek AMD



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (RSVD)

Size  
A 3

Document Number  
**Selek MLK AMD**


Date: Monday, December 16, 2019

Rev  
**A 00**

Sheet 22 of 106

(Blanking)

Selek AMD



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (RSVD)

Size  
A 3

Document Number  
**Selek MLK AMD**

Rev  
**A 00**

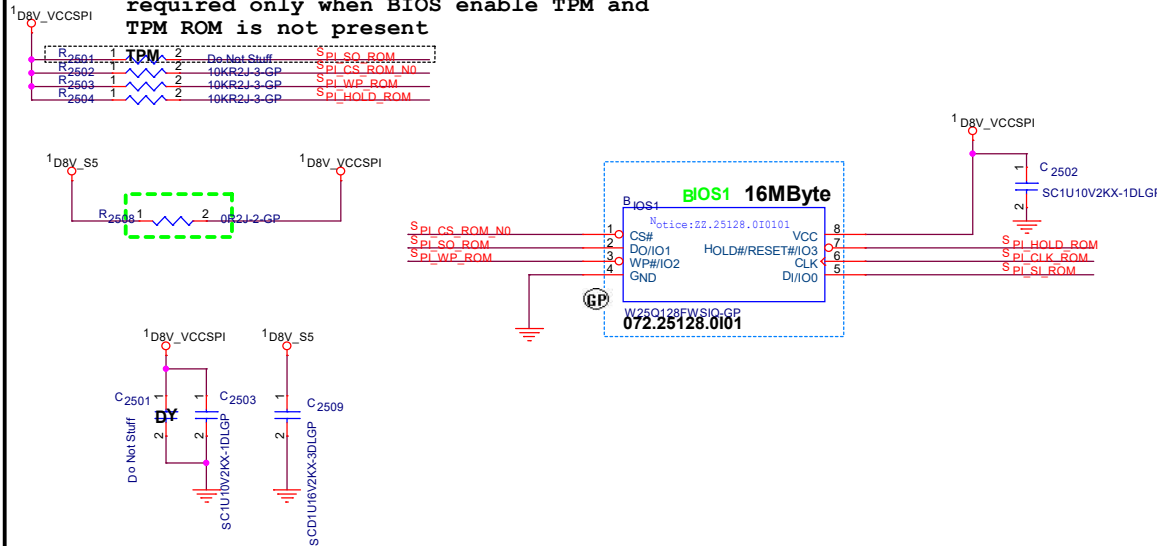
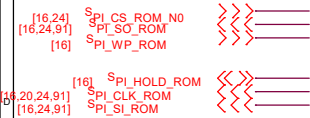
Date: Monday, December 16, 2019Sheet 23 of 106



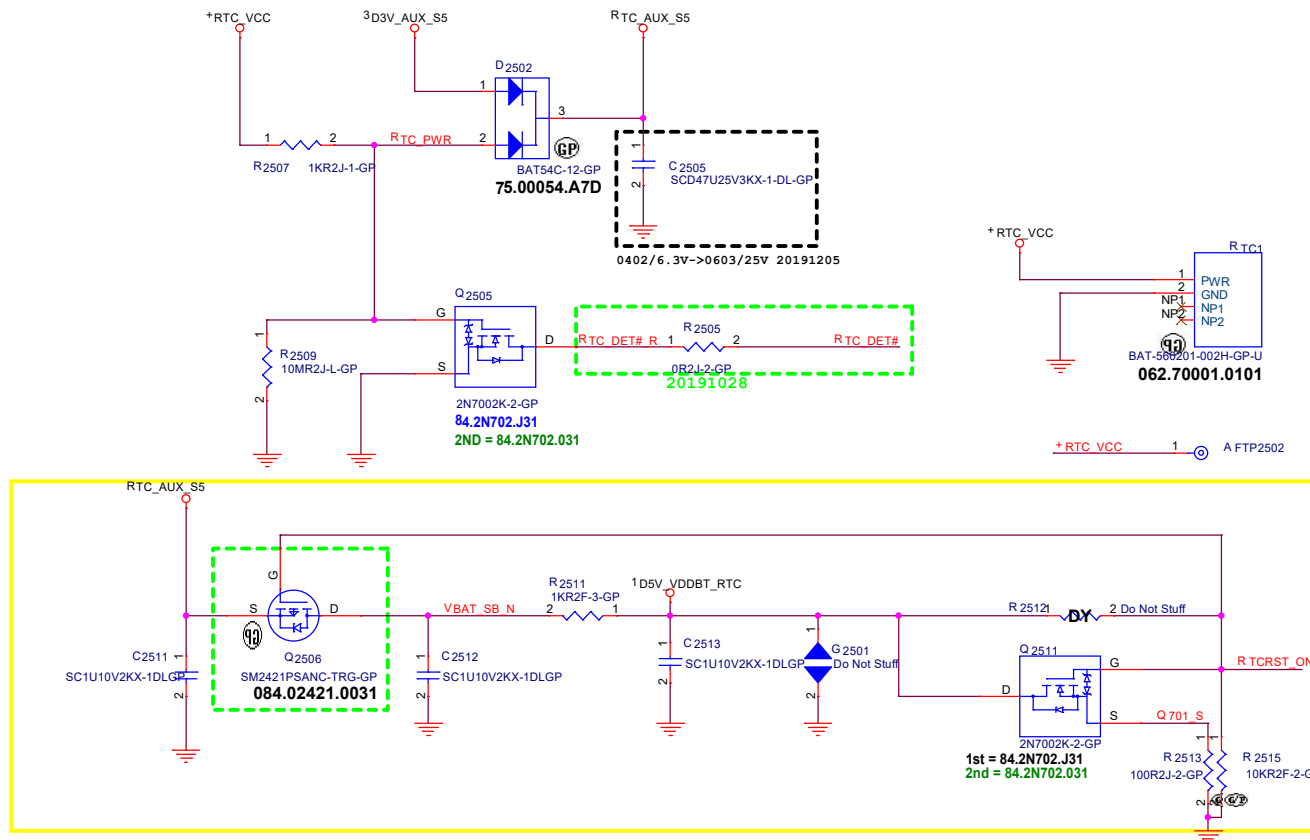
# SSID = Flash.ROM

required only when BIOS enable TPM and  
TPM ROM is not present

https://vinafix.com



# SSID = RBAT



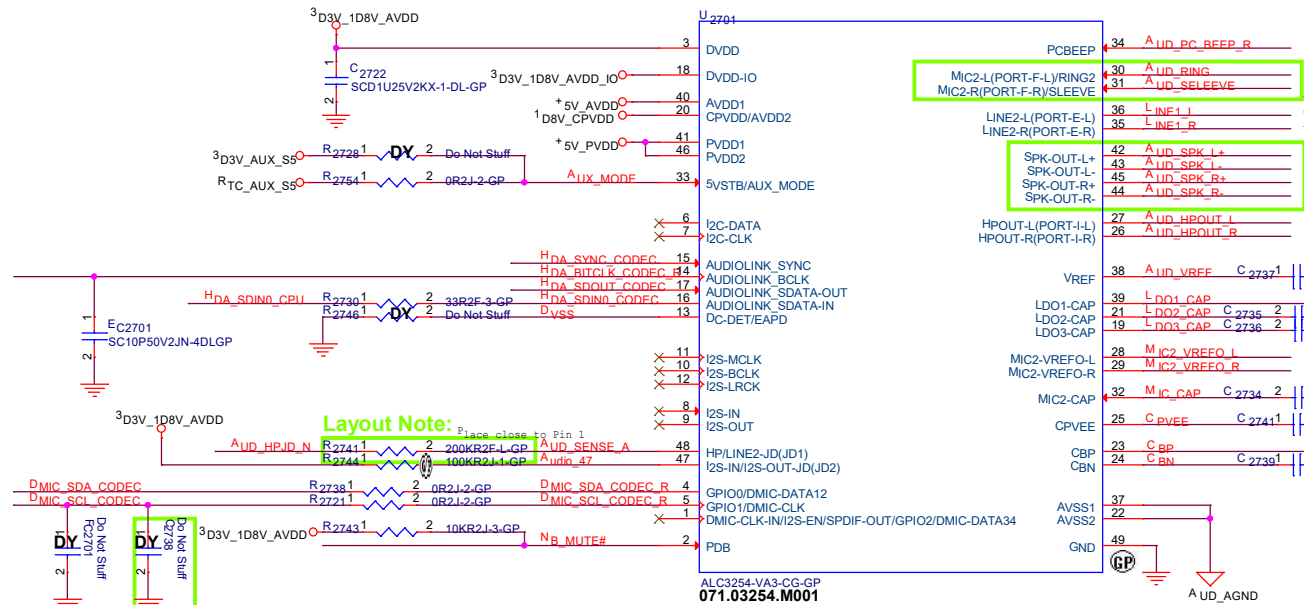
Selek AMD

<b>Wistron Corporation</b> 2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>FLASH / RTC</b>		
Size A3	Document Number <b>Selek MLK AMD</b>	Rev <b>A00</b>
Date: Monday, December 16, 2019 Sheet 25 of 106		



SSID = Audio

- [17] HDA\_SYNC\_CODEC >>>
- [17] HDA\_BITCLK\_CODEC\_R >>>
- [17] HDA\_SDOUT\_CODEC >>>
- [17] HDA\_SDIN0\_CPU <<<
- [55] DMIC\_SCL\_CODEC <<<
- [55] DMIC\_SDA\_CODEC <<<
- [17] SPKR >>>
- [24] BEEP >>>
- [29] MIC2\_VREF0\_L <<<
- [29] MIC2\_VREF0\_R <<<
- [29] AUD\_SPK\_L+ <<<
- [29] AUD\_SPK\_L- <<<
- [29] AUD\_SPK\_R+ <<<
- [29] AUD\_SPK\_R- <<<
- [29] AUD\_RING <<<
- [29] AUD\_SELEEVE <<<
- [29] LINE1\_L <<<
- [29] LINE1\_R <<<
- [29] AUD\_HPJD\_N <<<
- [24] NB\_MUTE# <<<
- [29] AUD\_HPOUT\_L <<<
- [29] AUD\_HPOUT\_R <<<

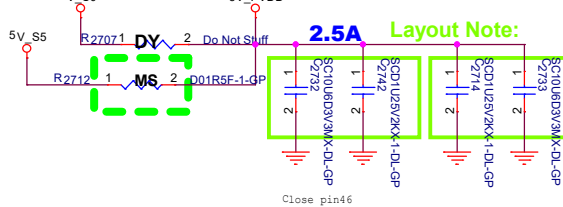
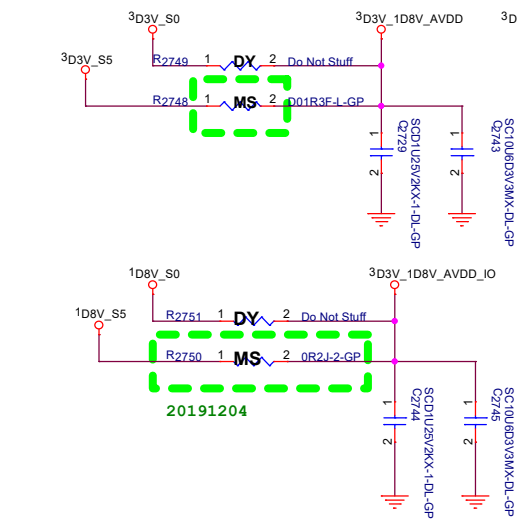


Layout Note: Place close to Pin 1

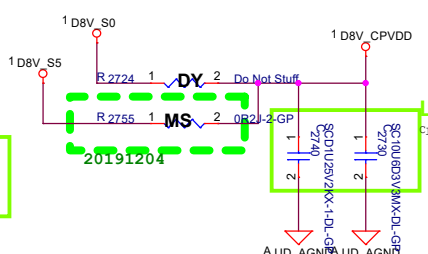
Layout Note: Width>40mil, to improve Headphone Crosstalk noise Change it to sharp will be better. Add 2 vias (>0.5A) when trace layer change.

Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

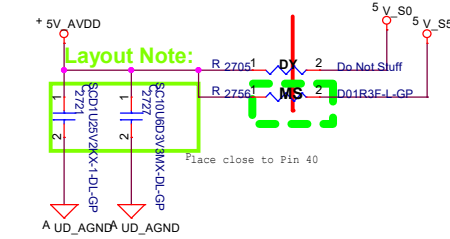
https://vinafix.com



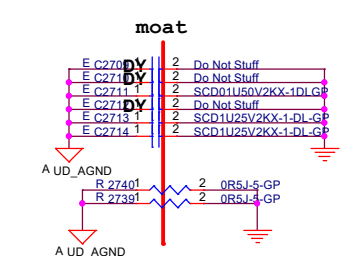
Layout Note: Close pin46



Layout Note: Close pin 20



Layout Note: Place close to Pin 40



Layout Note: R2739 should place nearby codec IC.

Selex AMD

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec ALC3254**

Size: A 3	Document Number: <b>Selek MLK AMD</b>	Rev: <b>X00</b>
Date: Monday, December 16, 2019	Sheet: 27 of 105	

(Blanking)

Selek AMD

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Audio</b>			
Size A4	Document Number <b>Selek MLK AMD</b>		Rev <b>A 00</b>
Date: Monday, December 16, 2019		Sheet 28	of 106

# Main Func = Audio

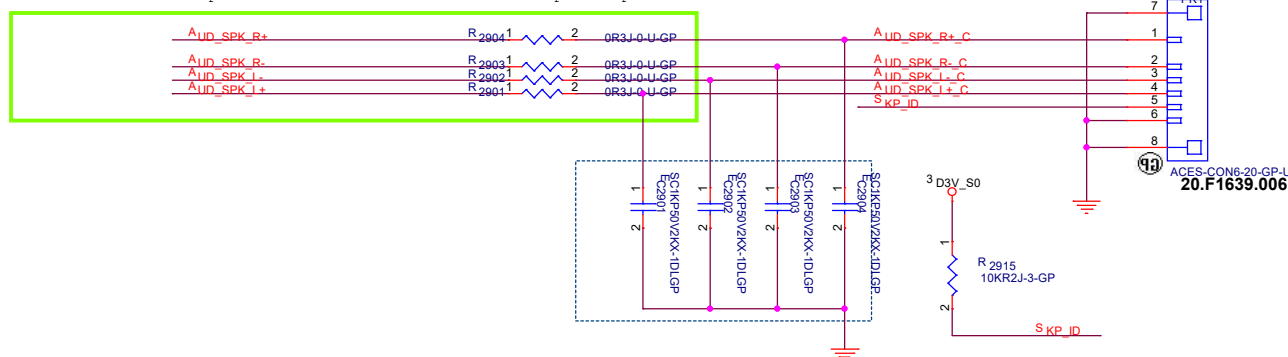
https://vinafix.com

[27] AUD\_SPK\_L+ >>>  
[27] AUD\_SPK\_L- >>>  
[27] AUD\_SPK\_R+ >>>  
[27] AUD\_SPK\_R- >>>

[17] SKP\_ID <<<

## Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

AUD\_SPK\_L\_ C 1 A FTP2901  
AUD\_SPK\_L+ C 1 A FTP2902  
AUD\_SPK\_R\_ C 1 A FTP2903  
AUD\_SPK\_R+ C 1 A FTP2904

## From Codec

[27] MIC2\_VREFO\_R >>>  
[27] MIC2\_VREFO\_L >>>

[27] AUD\_RING <<<

[27] AUD\_HPOUT\_L >>>

[27] LINE1\_L >>>

[27] AUD\_HPOUT\_R >>>

[27] LINE1\_R >>>

[27] AUD\_SELEEVE <<<

[27] AUD\_HPJD\_N <<<

## To IO Board

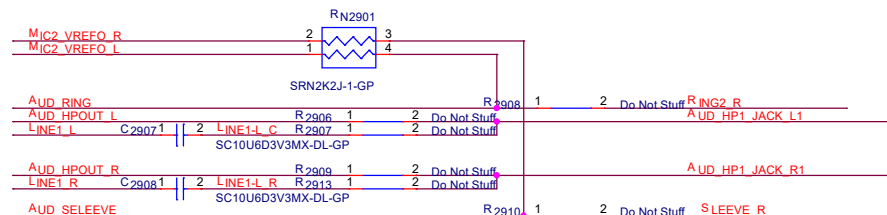
[66] RING2\_R <<<

[66] AUD\_HP1\_JACK\_L1 <<<

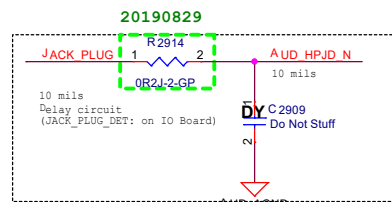
[66] JACK\_PLUG <<<

[66] AUD\_HP1\_JACK\_R1 <<<

[66] SLEEVE\_R <<<



## Universal Jack (Moved to I/O Board)



Selek AMD



Title		
Audio IO		
Size	Document Number	Rev
A3	Selek MLK_AMD	X00
Date:	Monday, December 16, 2019	Sheet 29 of 105

Main Func = Audio

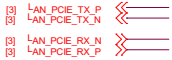
<https://vinafix.com>

(Blanking)

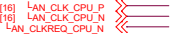
Selek AMD

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Selek MLK AMD</b>		Rev <b>A00</b>
Date: Monday, December 16, 2019		Sheet 30 of 106	

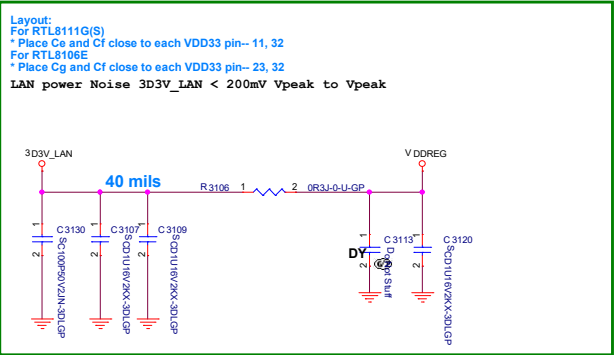
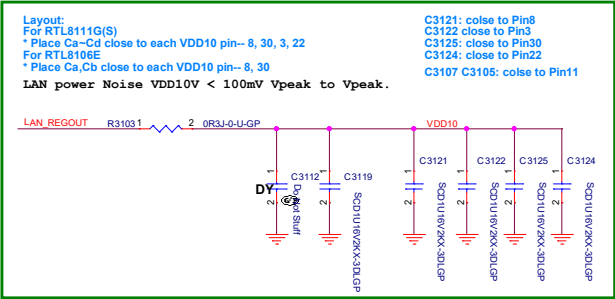
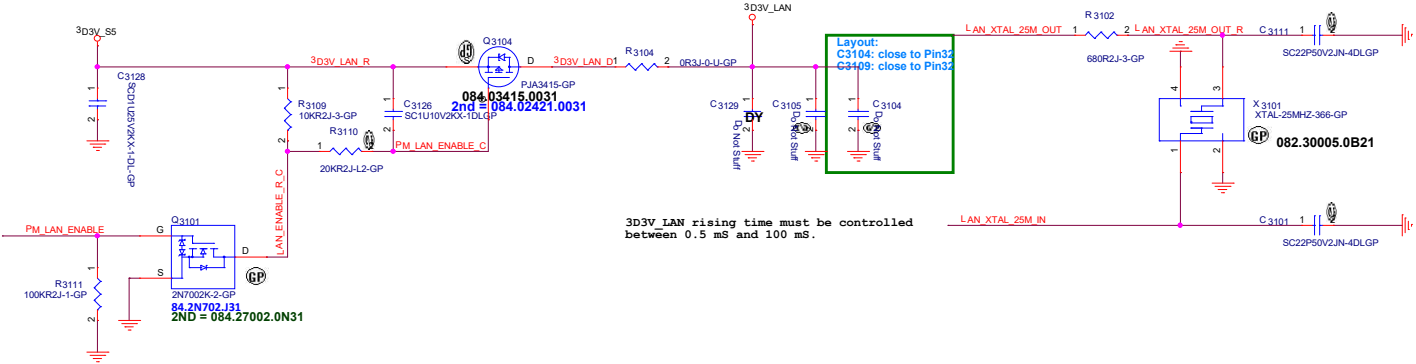
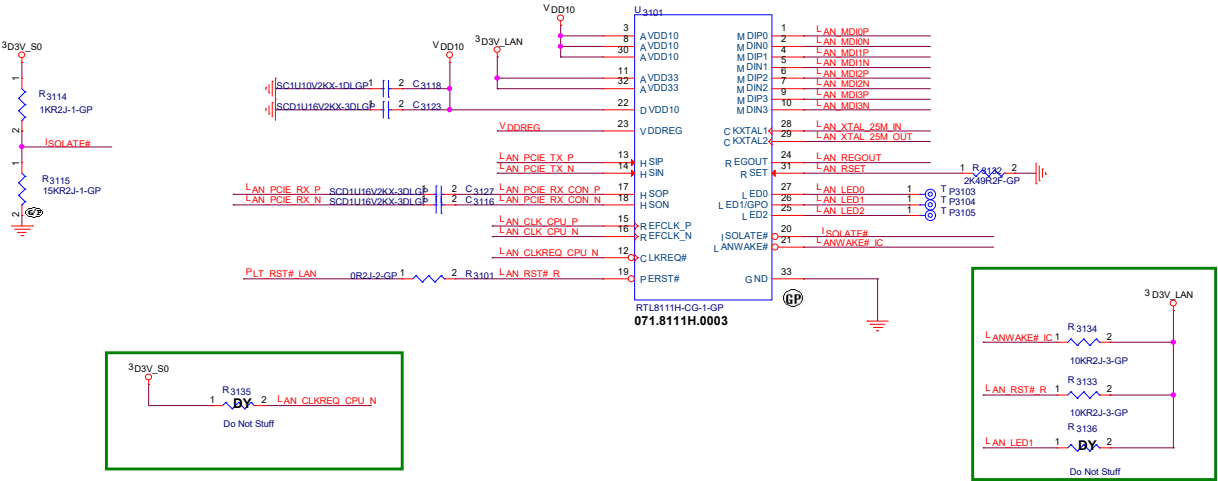
LAN



LAN\_CLK



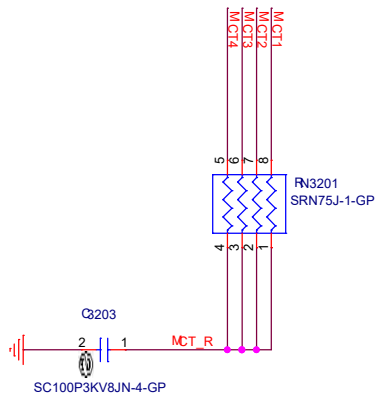
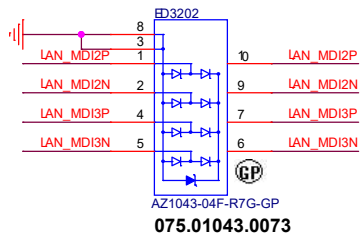
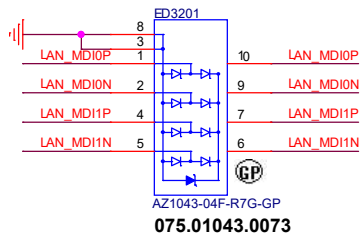
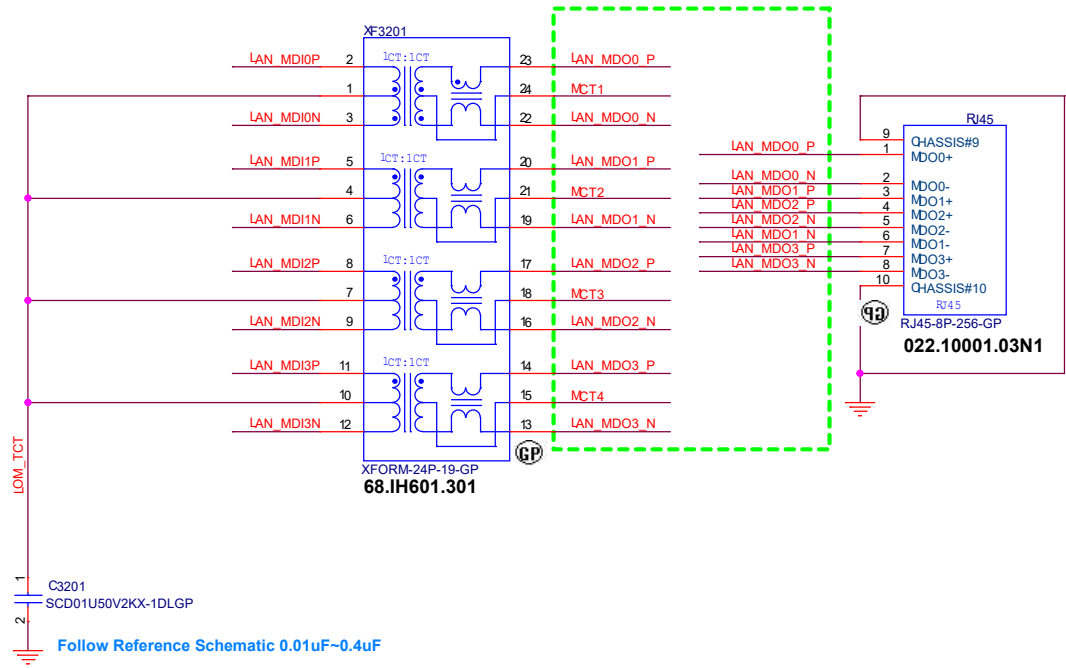
MDI



SSID = LAN

https://vinafix.com

[31] LAN\_MDI0P  
[31] LAN\_MDI0N  
[31] LAN\_MDI1P  
[31] LAN\_MDI1N  
[31] LAN\_MDI2P  
[31] LAN\_MDI2N  
[31] LAN\_MDI3P  
[31] LAN\_MDI3N



Selek AMD

**DELL** Wistron Corporation  
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **RJ45+Transformer**

Size B Document Number **Selek MLK AMD** Rev **A00**


Date: Monday, December 16, 2019 Sheet 1 of 105

Main Func = Card Reader

<https://vinafix.com>

(Blanking)

Selek AMD



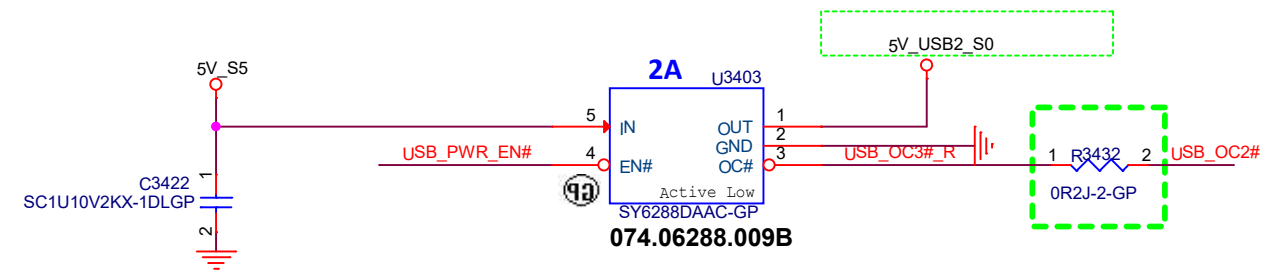
**Wistron Corporation**  
2 - 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan, R.O.C.

Title		
Card Reader-RTS5170		
Size	Document Number	Rev
A 3	Selek MLK AMD	A 00
Date: Monday, December 18, 2019		Sheet: 33 of 1
		108

Main Func = USB2.0

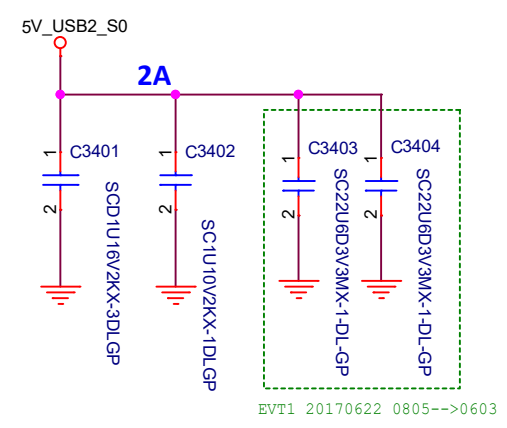
https://vinafix.com

2017.10.25  
Modify netname  
follow STD



USB2.0 Port2 (IO Board)


Layout Note: Close IO2



EVT1 20170622 0805-->0603

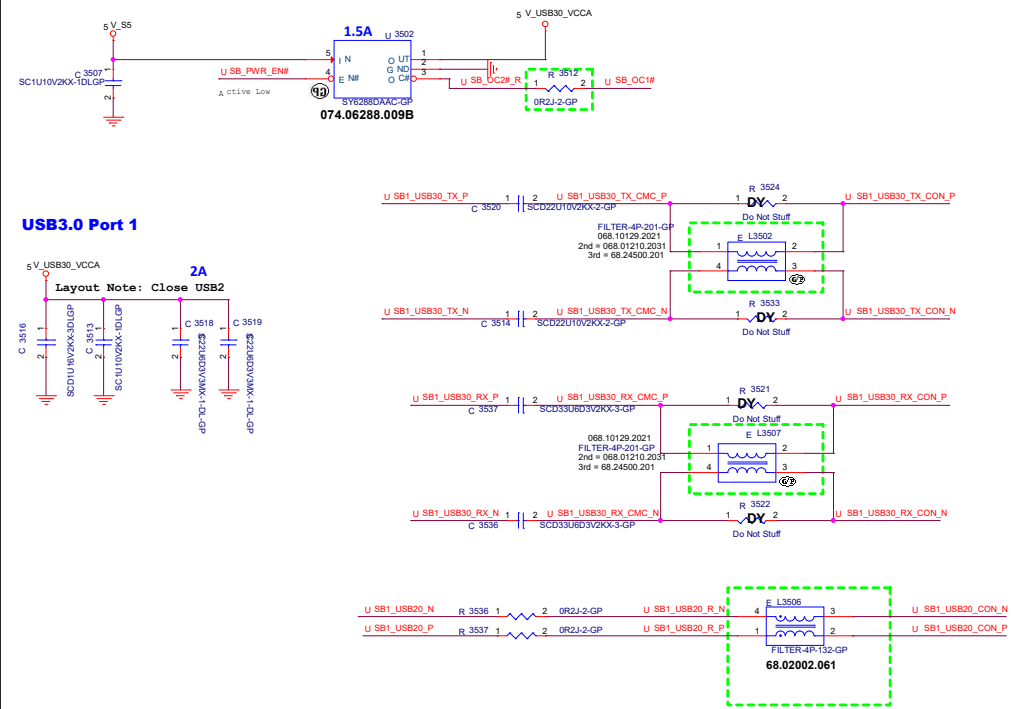
[18] USB\_OC2# <<< \_\_\_\_\_  
[24,35] USB\_PWR\_EN# >>> \_\_\_\_\_

Selek AMD

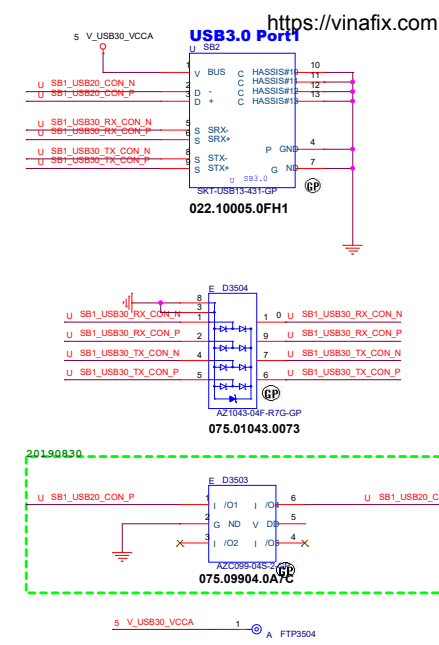
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>USB Charger</b>			
Size A4	Document Number <b>Selek MLK AMD</b>		Rev <b>A 00</b>
Date: Monday, December 16, 2019		Sheet 34 of 106	

Main Func = USB3.0 Port1

[18] uSB1\_USB30\_TX\_N >>>  
[18] uSB1\_USB30\_TX\_P >>>  
[18] uSB1\_USB30\_RX\_N <<<  
[18] uSB1\_USB30\_RX\_P <<<  
[18] uSB1\_USB20\_N <<<  
[18] uSB1\_USB20\_P <<<  
[24.34] uSB\_PWR\_ENH >>>  
[18] uSB\_OC1# <<<



Main Func = USB3.0 Port2




https://vinafix.com

Selek AMD

Main Func = USB Charger

<https://vinafix.com>

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Title <b>USB Charger</b>			
Size A4	Document Number <b>Selek MLK AMD</b>		Rev <b>A 00</b>
Date: Monday, December 16, 2019		Sheet 36	of 106

(Blanking)

Selek AMD



**Wistron Corporation**  
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipai Hsien 221, Taiwan, R.O.C.

Title

*Reserved*

Size A 3	Document Number <b>Selek MLK AMD</b>	Rev <b>A00</b>
-------------	---	-------------------

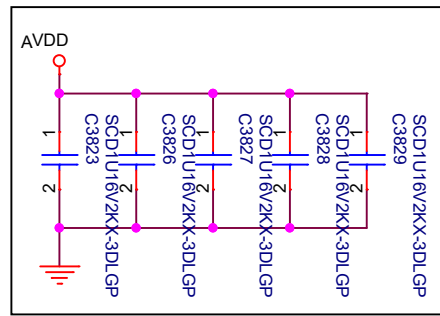
Date: Monday, December 16, 2019	Sheet 37 of 106
---------------------------------	-----------------

# Main Func = USB HUB

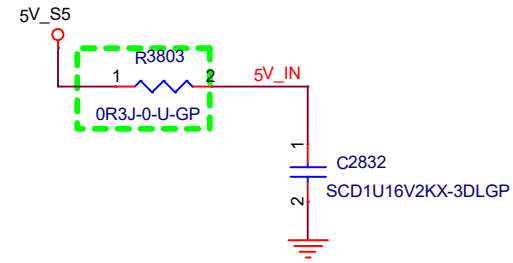
[18] HUB\_USB20\_P  
[18] HUB\_USB20\_N

[61] BT\_USB20\_P  
[61] BT\_USB20\_N

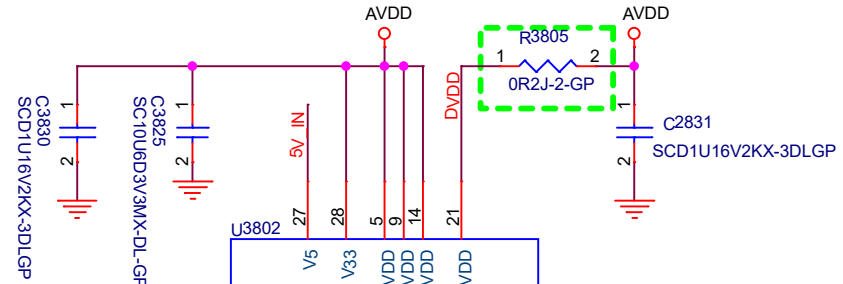
[65] RGB\_USB20\_P  
[65] RGB\_USB20\_N



Need to close the GL850G chip

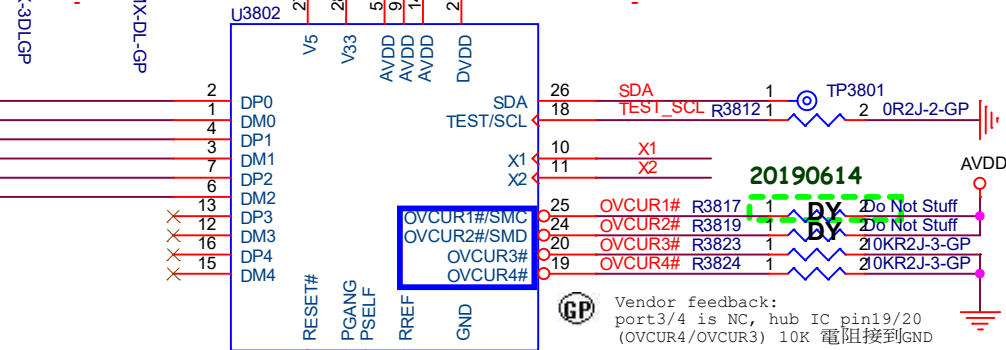


<https://vinafix.com>



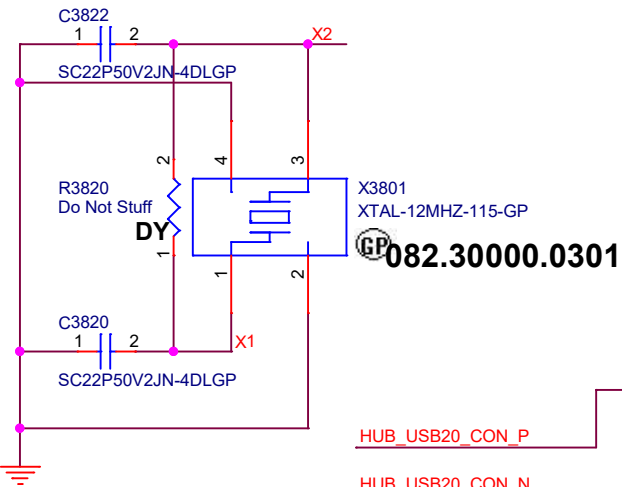
Bluetooth  
RGB

HUB\_USB20\_CON\_P  
HUB\_USB20\_CON\_N  
BT\_USB20\_P  
BT\_USB20\_N  
RGB\_USB20\_P  
RGB\_USB20\_N

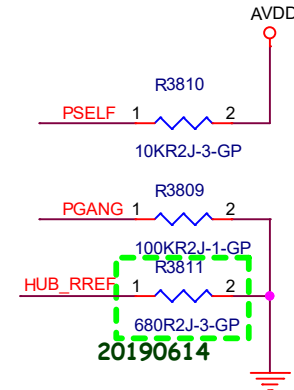
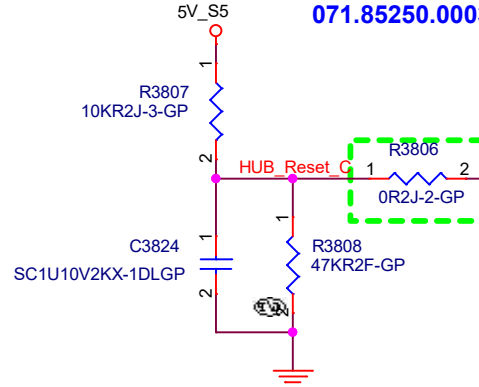


GL850G-OHY50-GP  
071.0850G.0003

BOM Change  
GL852G-50:  
071.85250.0003



082.30000.0301



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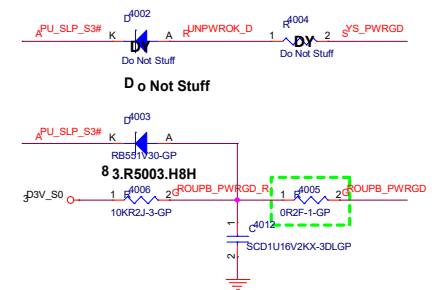
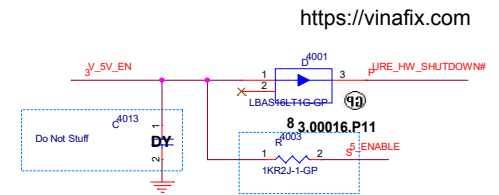
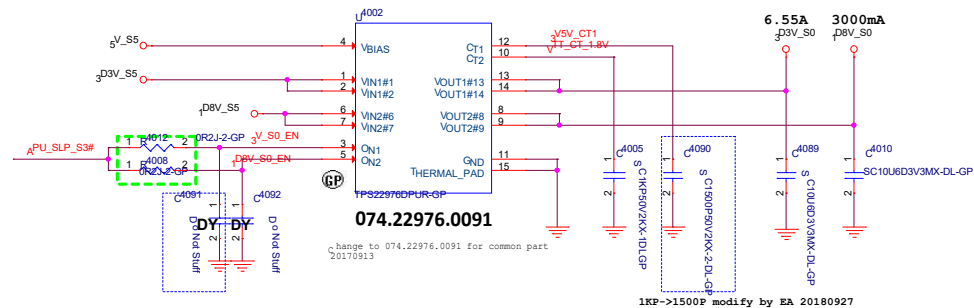
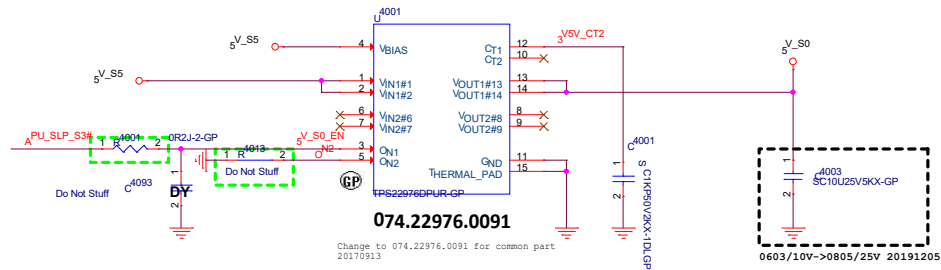
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB HUB</b>			
Size A4	Document Number		Rev
	<b>Selek MLK AMD</b>		<b>A00</b>
Date:	Monday, December 16, 2019	Sheet	38 of 106

Main Func = USB3.0 Port1

<https://vinafix.com>

# Power Sequence

[17,24,51,52,57,58,65] A\_PU\_SLP\_S3# >>>  
[45] 3\_V\_5V\_EN <<<  
[24,26] P\_URE\_HW\_SHUTDOWN# >>>  
[24] S\_5\_ENABLE >>>  
[17,24] S\_YS\_PWRGD >>>  
[44,46] C\_ROUPB\_PWRGD <<<



Delay for S0\_PWRGD to VCORE\_EN


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Main Func = Power Plane & Sequence

<https://vinafix.com>


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Title <b>Connected_Standby(1/2)+DS3</b>					
Size A4		Document Number <b>Selek MLK AMD</b>			Rev <b>A 00</b>
Date: Monday, December 16, 2019		Sheet 41		of 106	

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Connected\_Standby(2/2)

Size  
A 3

Document Number  
**Selek MLK AMD**

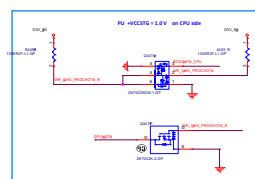
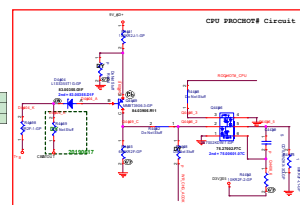
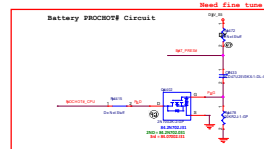
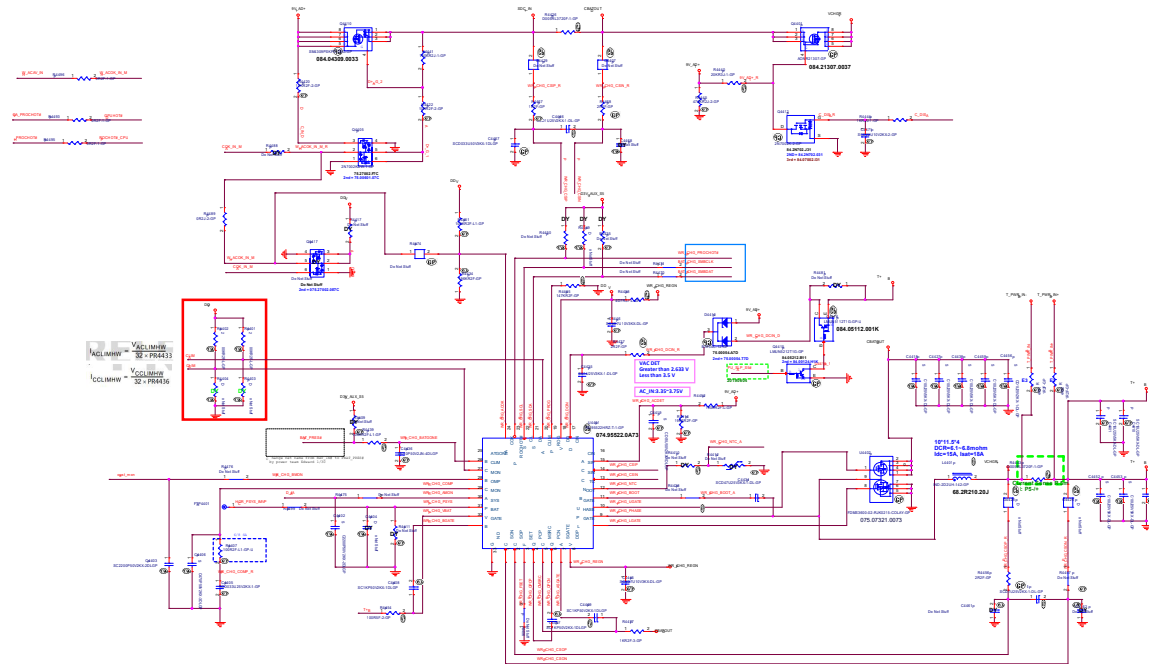
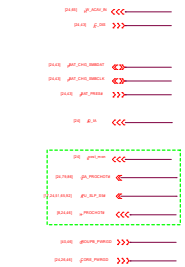
Rev  
**A 00**

Date: Monday, December 16, 2019Sheet 42 of 106

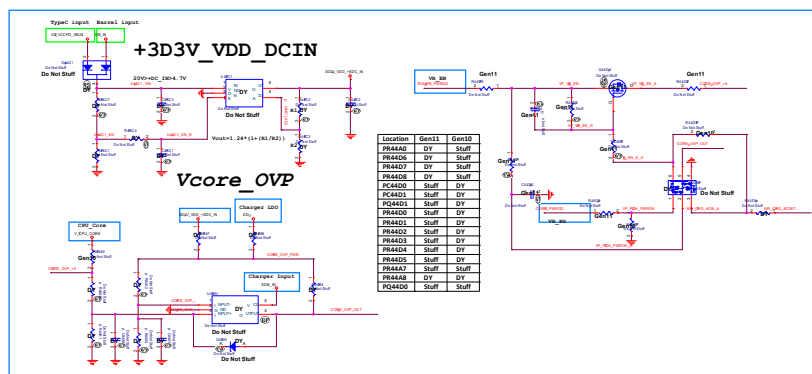


# ISL95522 Hybrid Charger

OFF PAGE

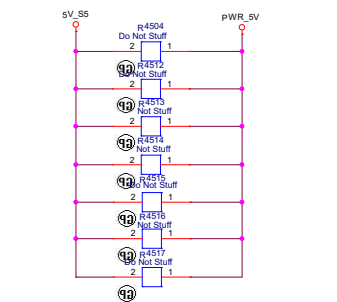
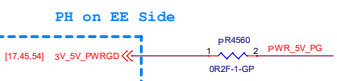


## OVP Circuit

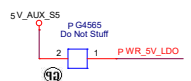
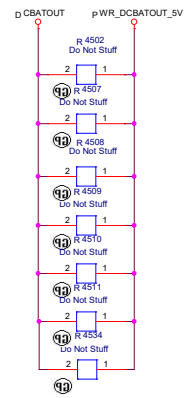


SSID = PWR.Plane.Regulator\_5V

OFFPAGE-Signal

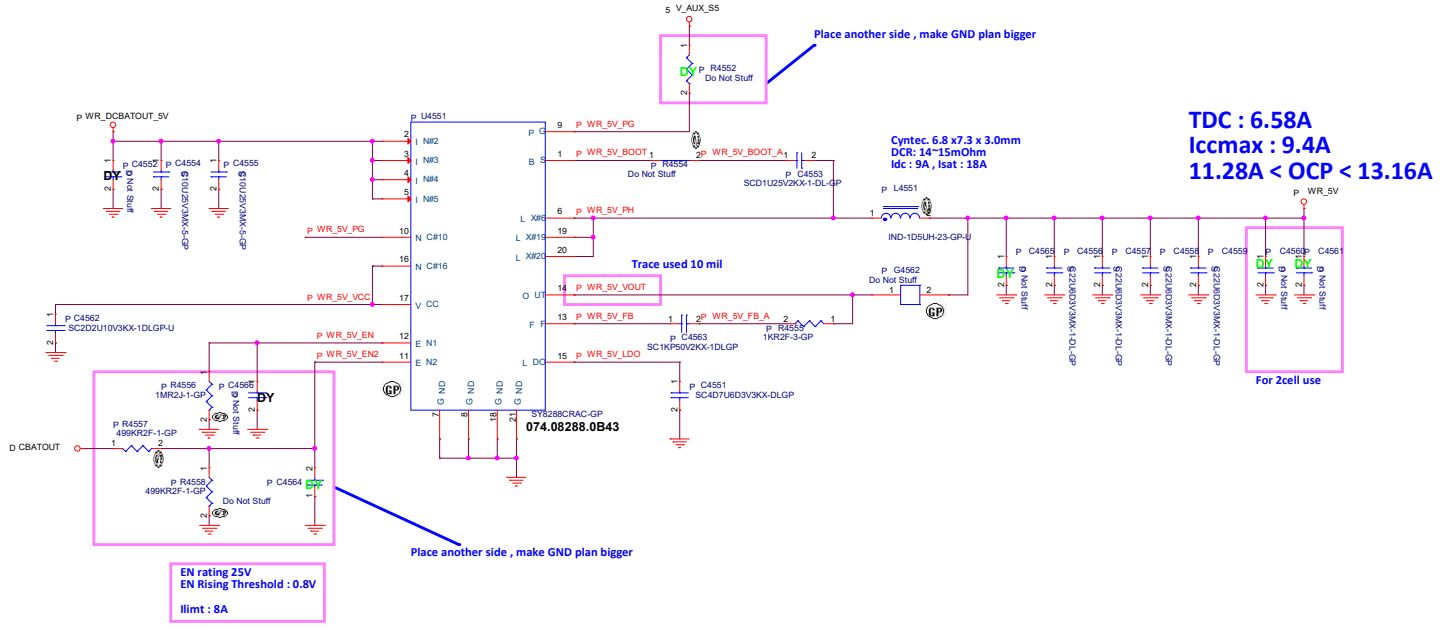


OFFPAGE-GAP



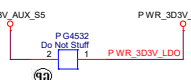
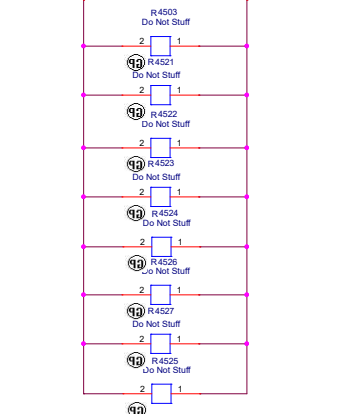
# SY8288C For 5V

https://vinafix.com

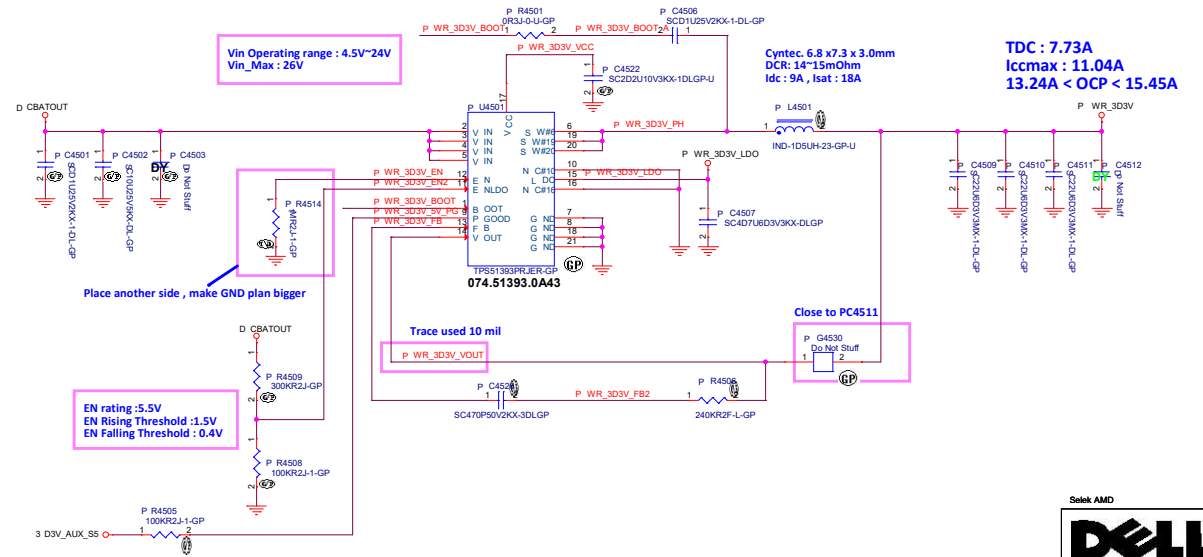


TDC : 6.58A  
Iccmax : 9.4A  
11.28A < OCP < 13.16A

SSID = PWR.Plane.Regulator\_3D3V

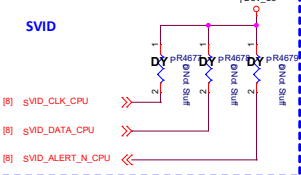


# TPS51393 For 3D3V



TDC : 7.73A  
Iccmax : 11.04A  
13.24A < OCP < 15.45A

## SVID



[47] pWR\_VCORE\_FCCM  
[47] pWR\_VCORE\_ISUMP  
[47] pWR\_VCORE\_ISUMN\_A

[47] pWR\_VCORE\_ISEN1  
[47] pWR\_VCORE\_ISEN2  
[47] pWR\_VCORE\_ISEN3

[47] pWR\_VCORE\_PWM1  
[47] pWR\_VCORE\_PWM2  
[47] pWR\_VCORE\_PWM3

[48] pWR\_VCORE\_PWM\_SOC  
[48] pWR\_VCORE\_FCCM\_SOC  
[48] pWR\_VCORE\_VO\_SOC  
[48] pWR\_VCORE\_ISUMP\_SOC

[R24,44] V\_PROCHOT#  
[40,44] GROUP\_PWRGD

## VDDSOC SENSE

[8] VCCSOC\_SENSE  
[8] VSSSOC\_SENSE

## VCORE SENSE

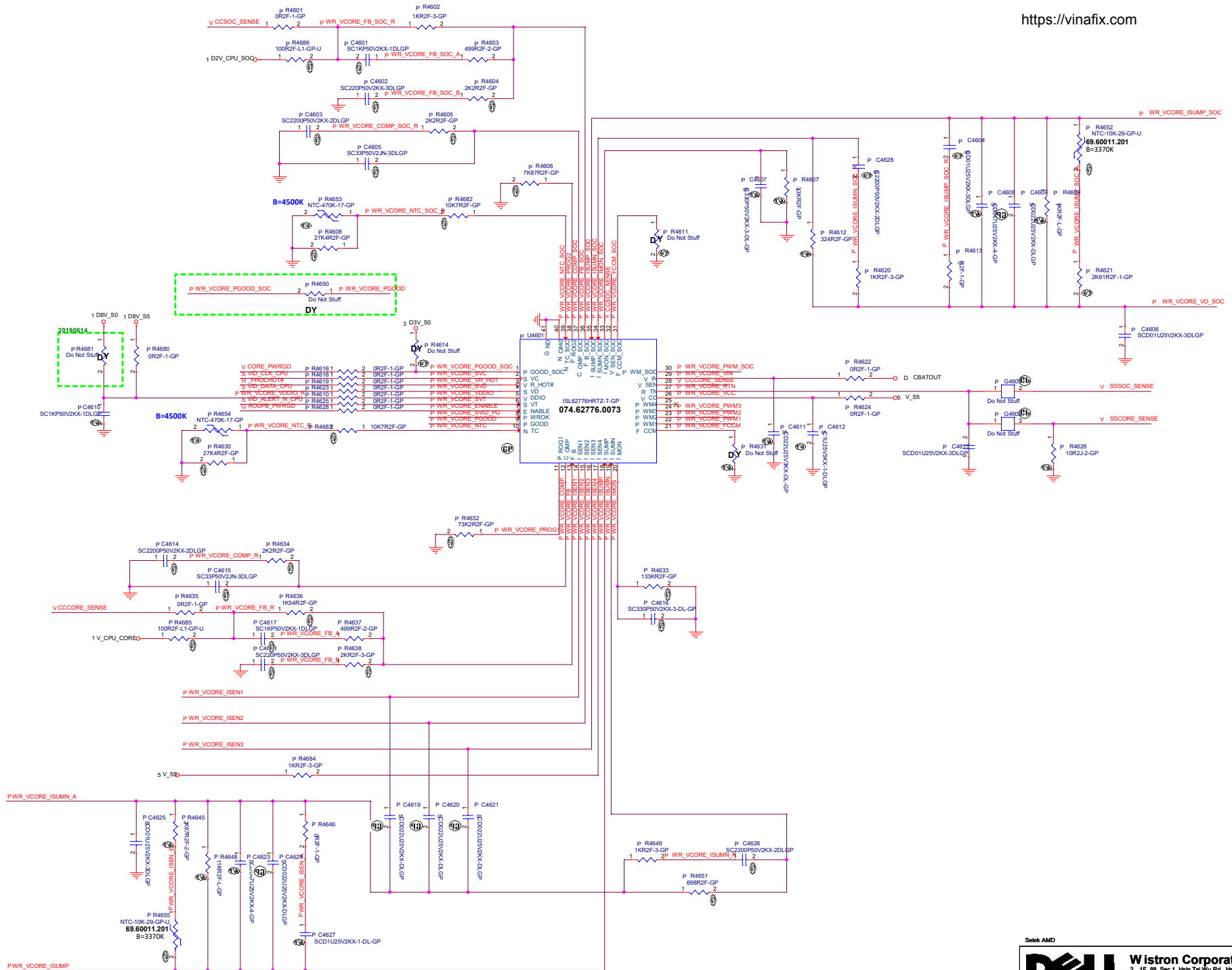
[8] VCCCORE\_SENSE  
[8] VSSCORE\_SENSE

## SVID\_PG

[8,68] SVID\_PWRGD

## VDD\_PG

[24,26,44] VCORE\_PWRGD




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Size A4	Document Number <b>Selek MLK AMD</b>		Rev <b>A 00</b>
Date: Monday, December 16, 2019		Sheet 49 of	14

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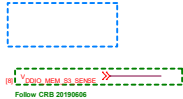
Selek AMD

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Reserved</b>					
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Date: Monday, December 16, 2019		Sheet 50		of 14	

# OFFPAGE



PH on EE Side

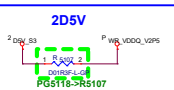
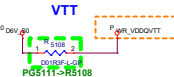
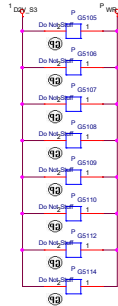


# OFFPAGE\_GAP



Current Sense R:10m

CH: P74+



20190808

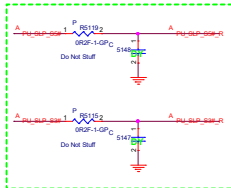
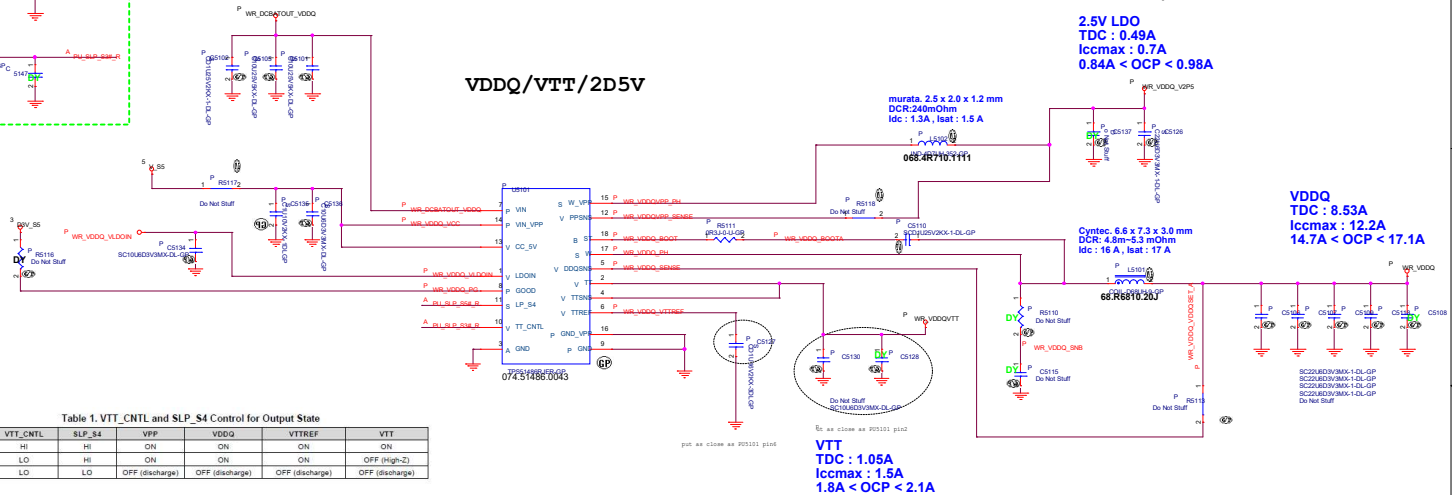


Table 1. VTT\_CNTL and SLP\_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VFP	VDDQ	VTTREF	VIT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (high-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

# VDDQ/VTT/2D5V

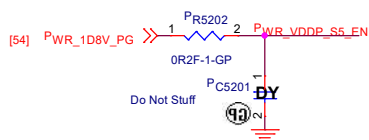


https://vinafix.com

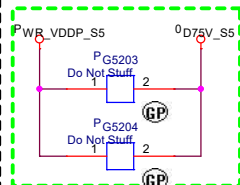
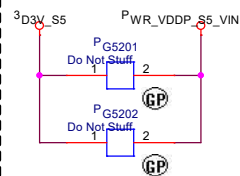
SSID = PWR.Plane.Regulator\_VDDP

OFFPAGE-Signal

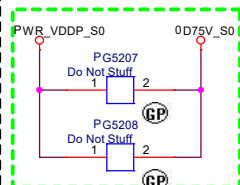
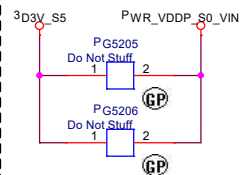
PH on EE Side



OFFPAGE-GAP

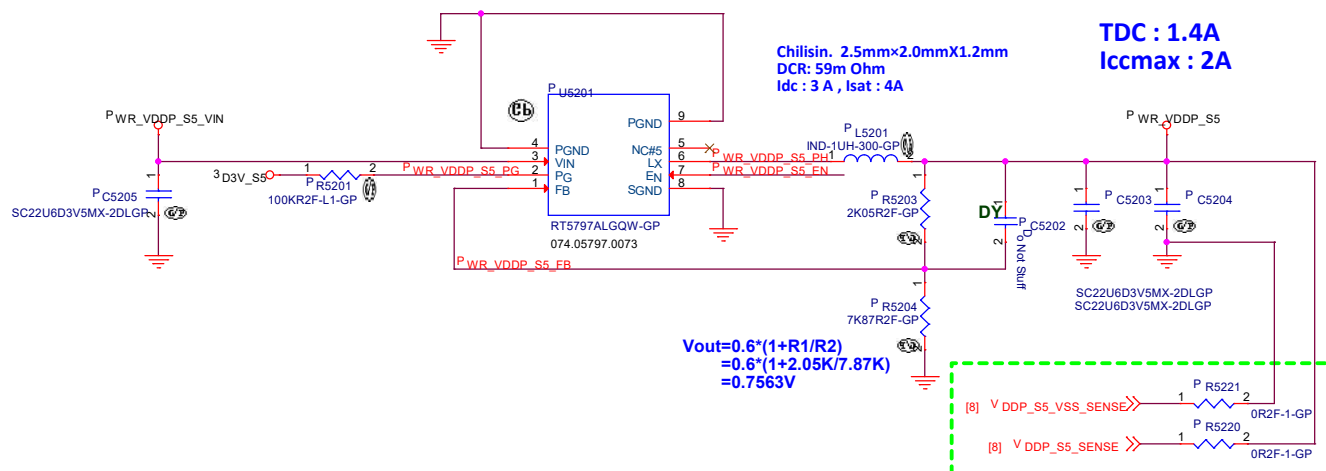


PH on EE Side

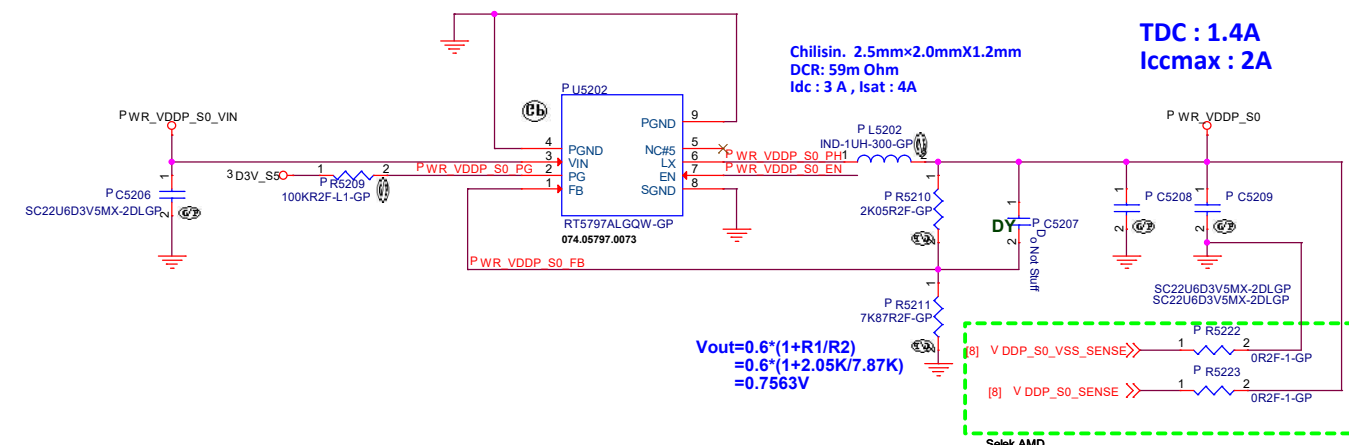


VDDP\_S5

https://vinafix.com



VDDP\_S0



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Date: Monday, December 16, 2019		Sheet 53		of 14	



# Main Func = LCD

[14] >>> DP\_AUX\_CPU\_N <<<  
 [14] >>> DP\_AUX\_CPU\_P <<<  
 [14] >>> DP\_TX\_CPU\_N <<<  
 [14] >>> DP\_TX\_CPU\_P <<<  
 [14] >>> DP\_TX\_CPU\_N1 <<<  
 [14] >>> DP\_TX\_CPU\_P1 <<<  
 [14] >>> DP\_TX\_CPU\_N2 <<<  
 [14] >>> DP\_TX\_CPU\_P2 <<<  
 [14] >>> DP\_TX\_CPU\_N3 <<<  
 [14] >>> DP\_TX\_CPU\_P3 <<<

[14] >>> JRC\_PANEL\_N <<<  
 [14] >>> LCD\_TEST <<<  
 [14] >>> D\_ON\_OUT <<<  
 [14] >>> DP\_HPO\_CPU <<<

[14] >>> LCD\_BRIGHTNESS <<<  
 [14] >>> LCD\_TEST\_EN <<<

[14] >>> DP\_VARY\_BL <<<  
 [14] >>> DP\_DCON <<<

KBC 20190606  
 [14] >>> PANEL\_MONITOR <<<

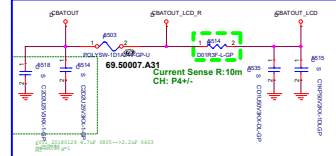
# Main Func = CAMERA

[14] >>> CCD\_USB2\_N <<<  
 [14] >>> CCD\_USB2\_P <<<

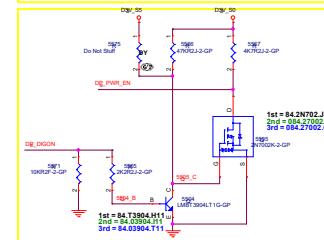
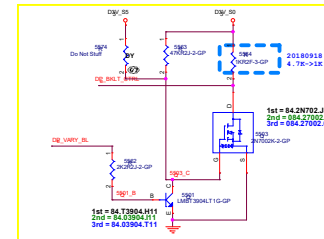
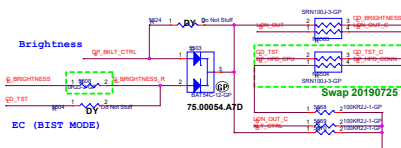
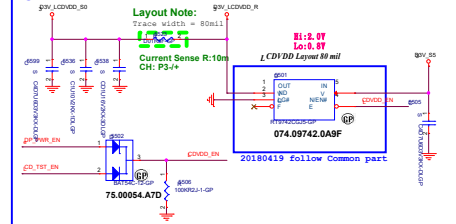
[17] >>> DMC\_SDA\_CODEC <<<  
 [17] >>> DMC\_SCL\_CODEC <<<  
 [17] >>> DMC\_DATA\_ESP <<<  
 [17] >>> DMC\_CLK\_ESP <<<

# Main Func = Touch panel

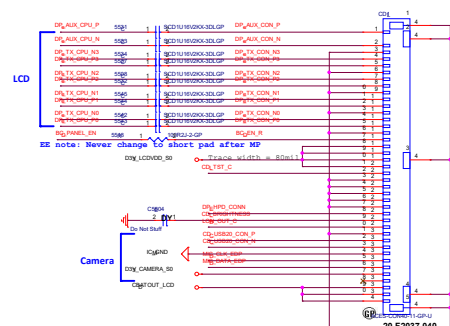
## INVERTER POWER



## LCDVDD



<https://vinafix.com>



Layout Note:

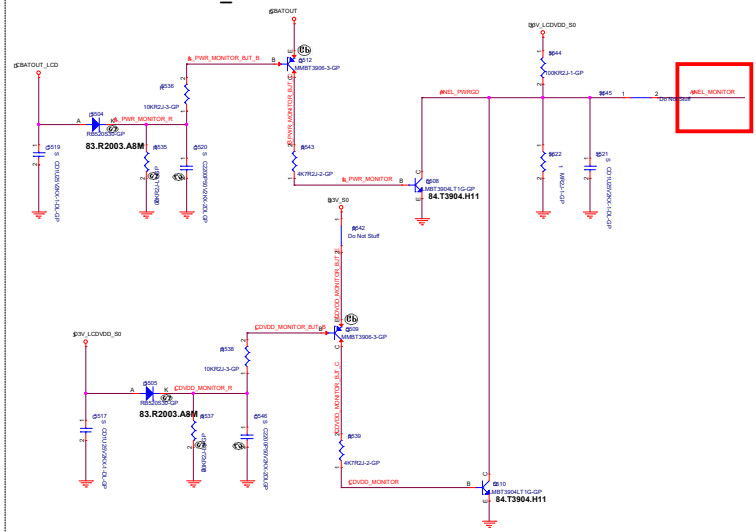
Colim to LCD1

100k

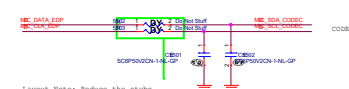
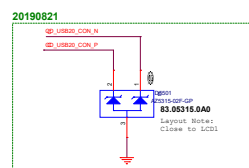
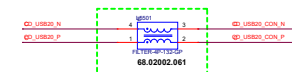
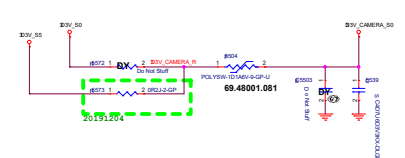
## PU/PD FOR AUX CHANNEL

PU/PD (PULL-UP):  
 The circuit includes a pull-up resistor of 100k for AUXN and a pull-down resistor of 100k for AUXP between the I2C detector and the connector, to assist source detection by the aux device.

## PANEL\_PWRGD CIRCUIT



## CAMERA POWER



## Touch Panel

(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT

Size

A 3

Document Number

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Rev

A 00

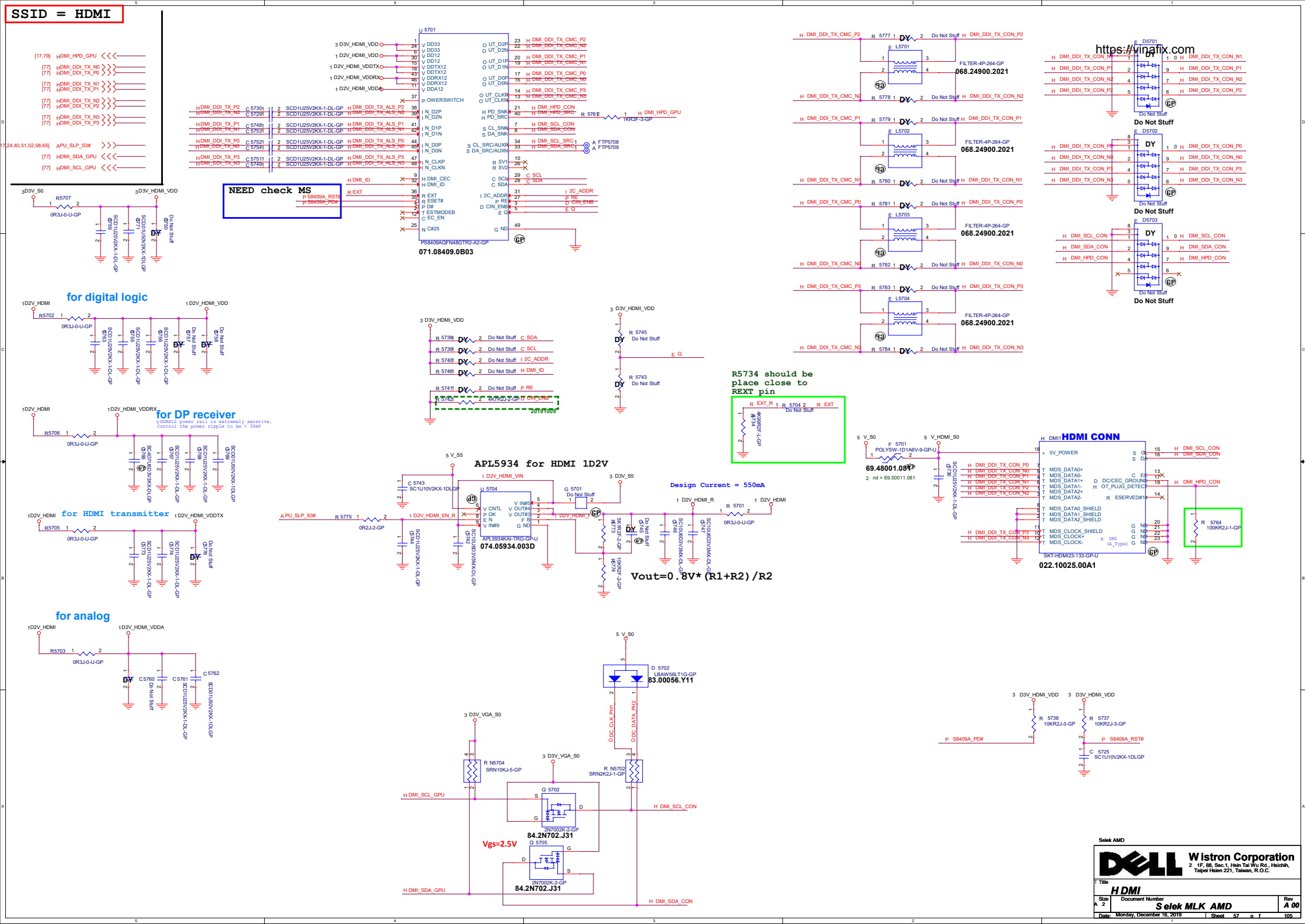
Date

Monday, December 18, 2018

Sheet


58 of 1

108





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Title <b>(Reserved)</b>			
Size A 3	Document Number <b>Selek MLK AMD</b>		Rev <b>A00</b>
Date: Monday, December 16, 2019		Sheet 59 of	106

Main Func = HDD

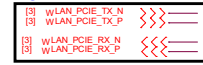
<https://vinafix.com>

Selek AMD

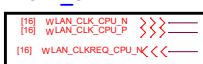
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>SATA IF HDD/ODD</b>					
Size A 3	Document Number				Rev
<b>Selek MLK AMD</b>				<b>A 00</b>	
Date:	Monday, December 16, 2019			Sheet	60 of 106

Main Func = WLAN

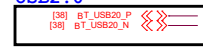
PCIE



PCIE\_CLK



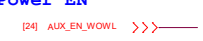
USB2.0



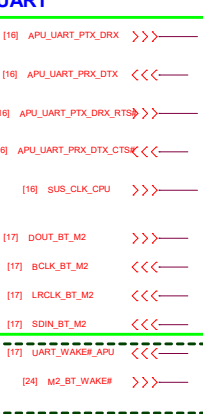
Single end



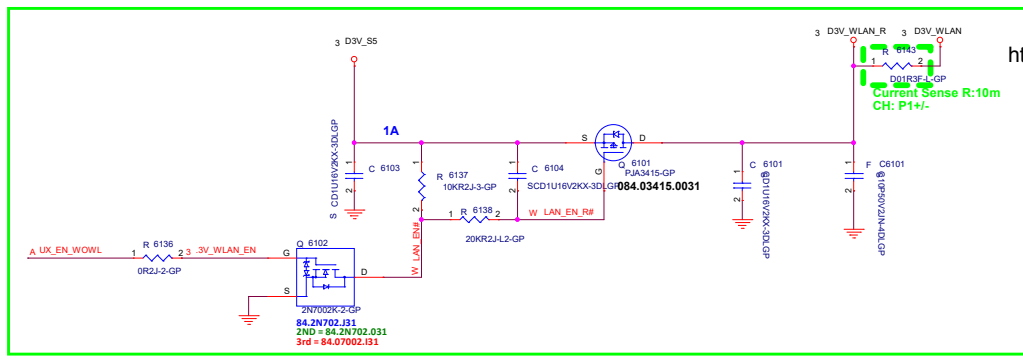
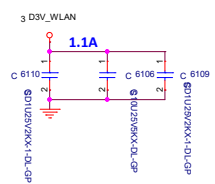
Power EN



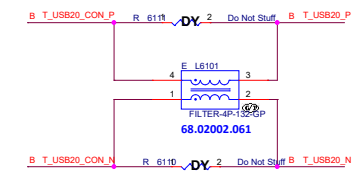
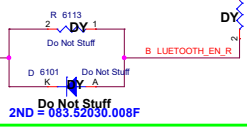
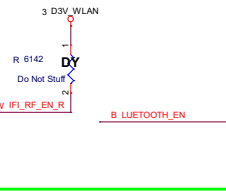
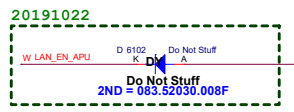
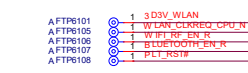
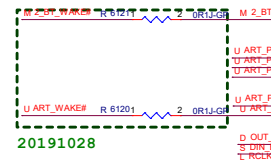
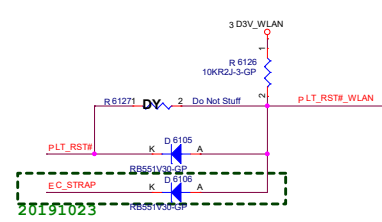
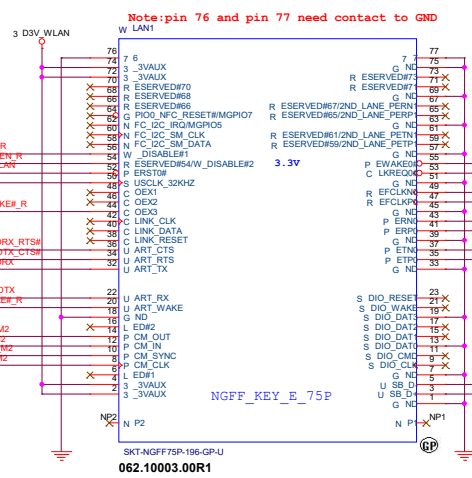
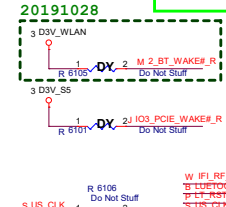
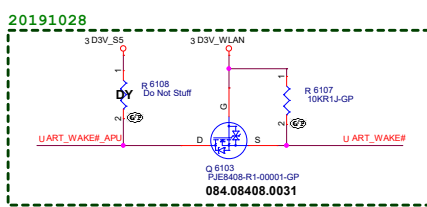
UART



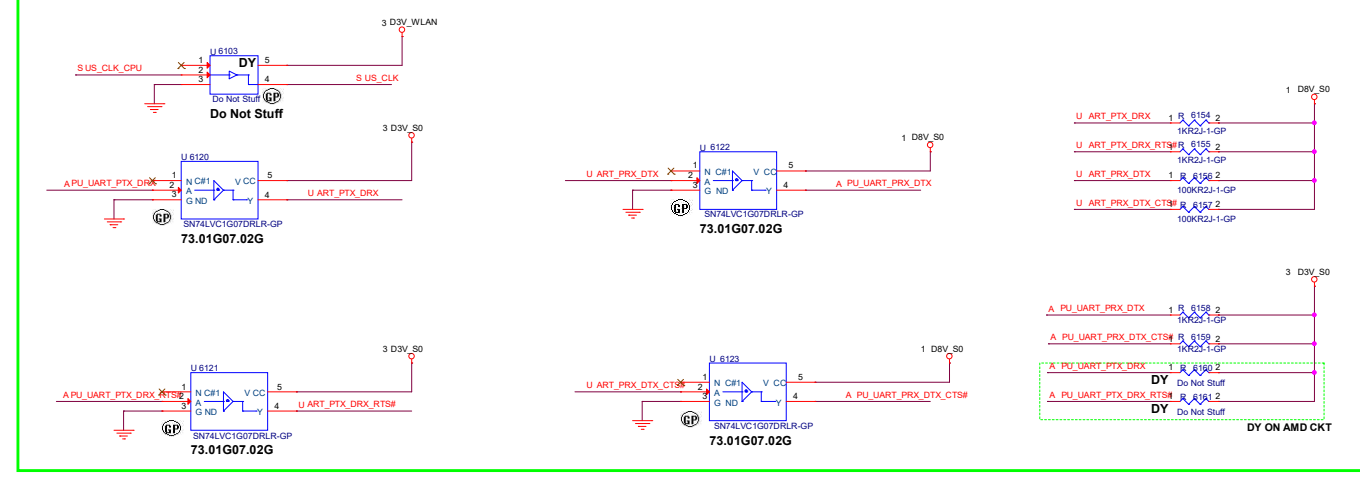
20191028



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20191028 UART Device for WLAN



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Title			
<b>Reserved</b>			
Size A4	Document Number <b>Selek MLK AMD</b>		Rev <b>A 00</b>
Date: Monday, December 16, 2019		Sheet 62 of	106

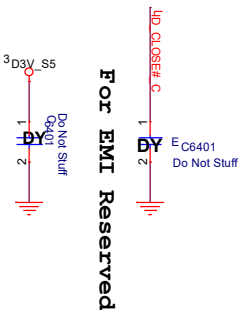
[3] SSD\_PCIE\_RX\_N11  
[3] SSD\_PCIE\_RX\_P11  
[3] SSD\_PCIE\_TX\_N11  
[3] SSD\_PCIE\_TX\_P11

Title			<b>INT 10 (SSD M.2)</b>		
Size A 2	Document Number <b>Selek MLK AMD</b>				Rev A
Date: Monday, December 16, 2019			Sheet 63 of 106		

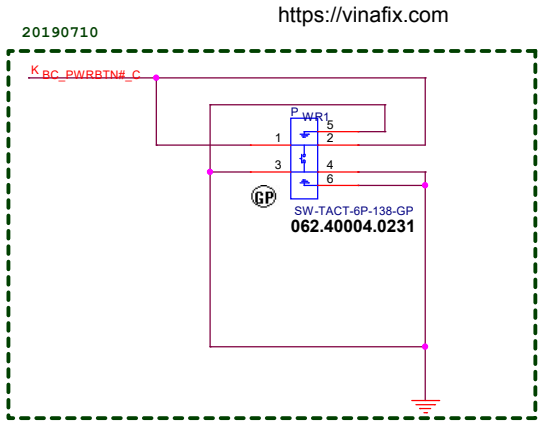
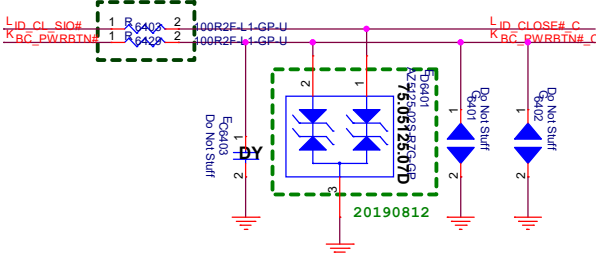
Main Func = Power BTN

[24,65] L\_ID\_CL\_SIO# <<< \_\_\_\_\_  
[24] K\_BC\_PWRBTN# <<< \_\_\_\_\_  
[66,92] L\_ID\_CLOSE#\_C >>> \_\_\_\_\_  
[92] K\_BC\_PWRBTN#\_C <<< \_\_\_\_\_

Low actived from KBC GPIO



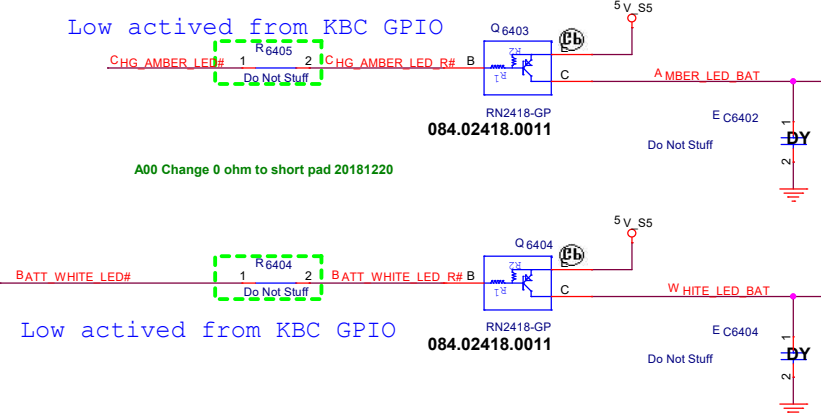
Power button



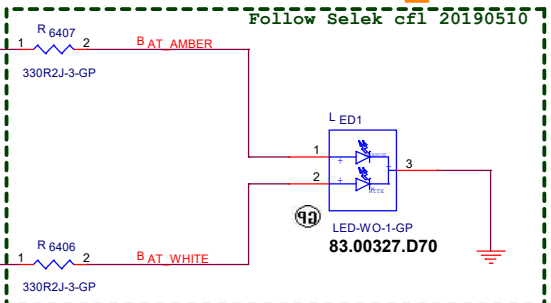
Main Func = Battery LED

[24] CHG\_AMBER\_LED# >>> \_\_\_\_\_  
[24] BATT\_WHITE\_LED# >>> \_\_\_\_\_

Low actived from KBC GPIO



Battery LED1 (AMBER\_LED)

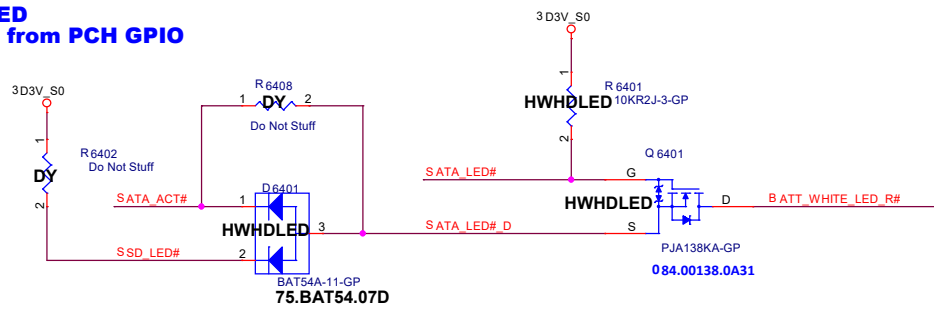


Battery LED2 (WHITE\_LED)

Main Func = SATA LED

[17] SATA\_ACT# >>> \_\_\_\_\_  
[24,64] SATA\_LED# >>> \_\_\_\_\_  
[24,64] SATA\_LED# >>> \_\_\_\_\_  
[63] SSD\_LED# >>> \_\_\_\_\_

SATA HDD LED  
LOW actived from PCH GPIO



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Title: **LED Board&Power Button**

Size A 3	Document Number <b>Selek MLK_AMD</b>	Rev <b>A 00</b>
Date: Monday, December 16, 2019	Sheet 64 of 106	



Main Func = IO Connector

USB2.0



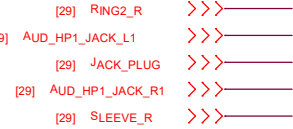
Card Reder



I2C

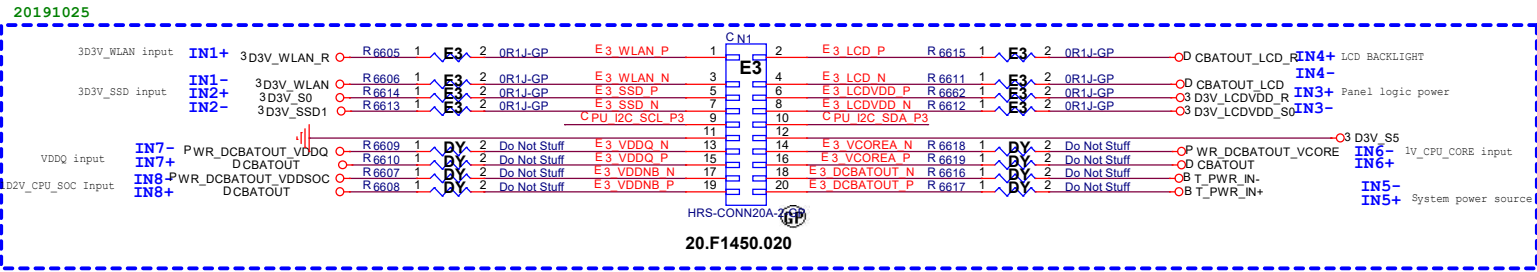
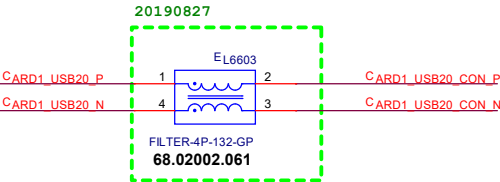
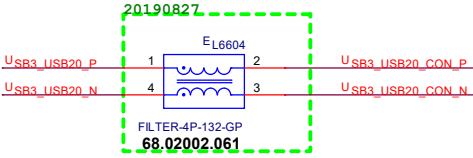
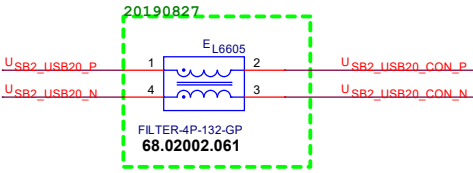
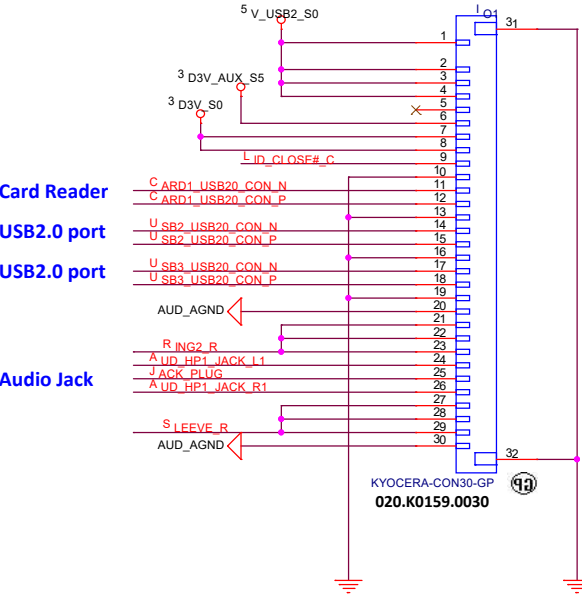


Audio Jack



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I/O Board Connector



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Title IO Board Connector

Size A3 Document Number Selelk MLK AMD Rev A00

Date: Monday, December 16, 2019 Sheet 66 of 106

5 4 3 2 1

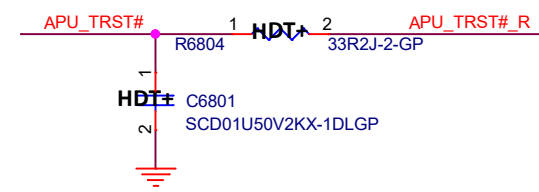
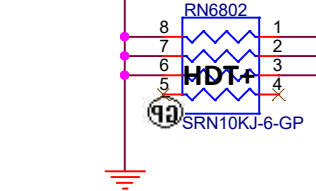
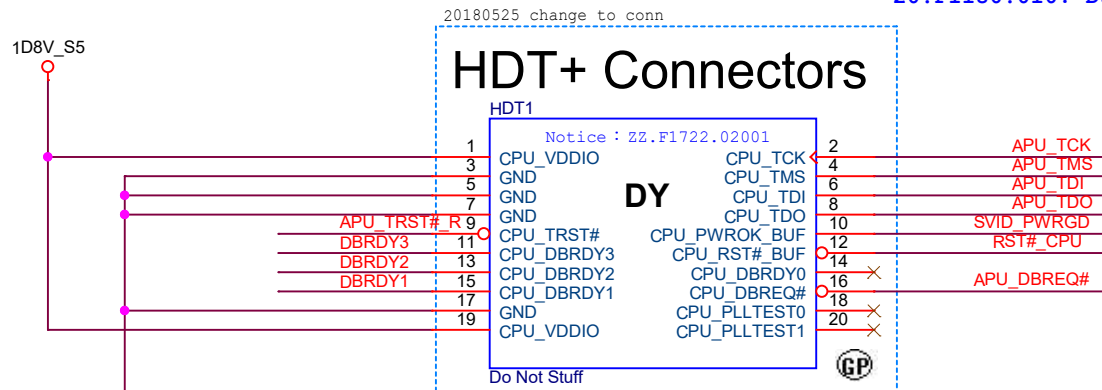
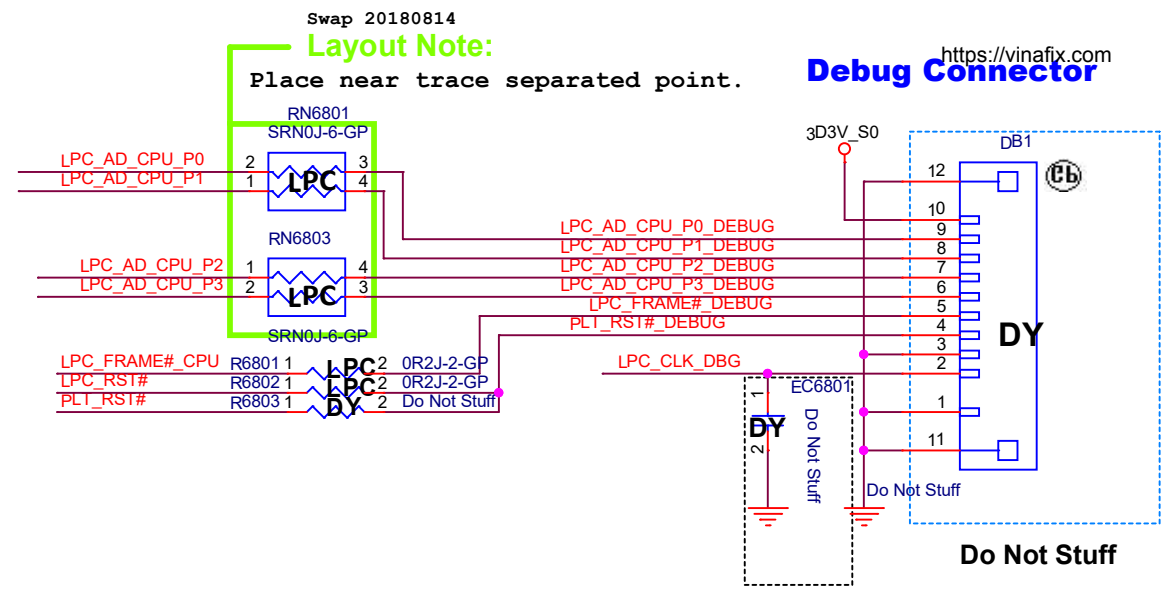
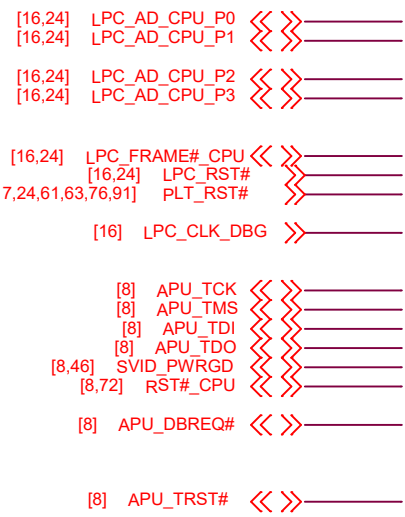
**Main Func = HALL SENSOR**

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<b>Reserved</b>			
Size A4	Document Number <b>Selek MLK AMD</b>		Rev <b>SB</b>
Date: Monday, December 16, 2019		Sheet 67 of	105

SSID = DEBUG PORT



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Title **Dubug connector**


Size A4	Document Number <b>Selek MLK AMD</b>	Rev <b>A00</b>
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Date: Monday, December 16, 2019 Sheet 68 of 106

Sensor HUB

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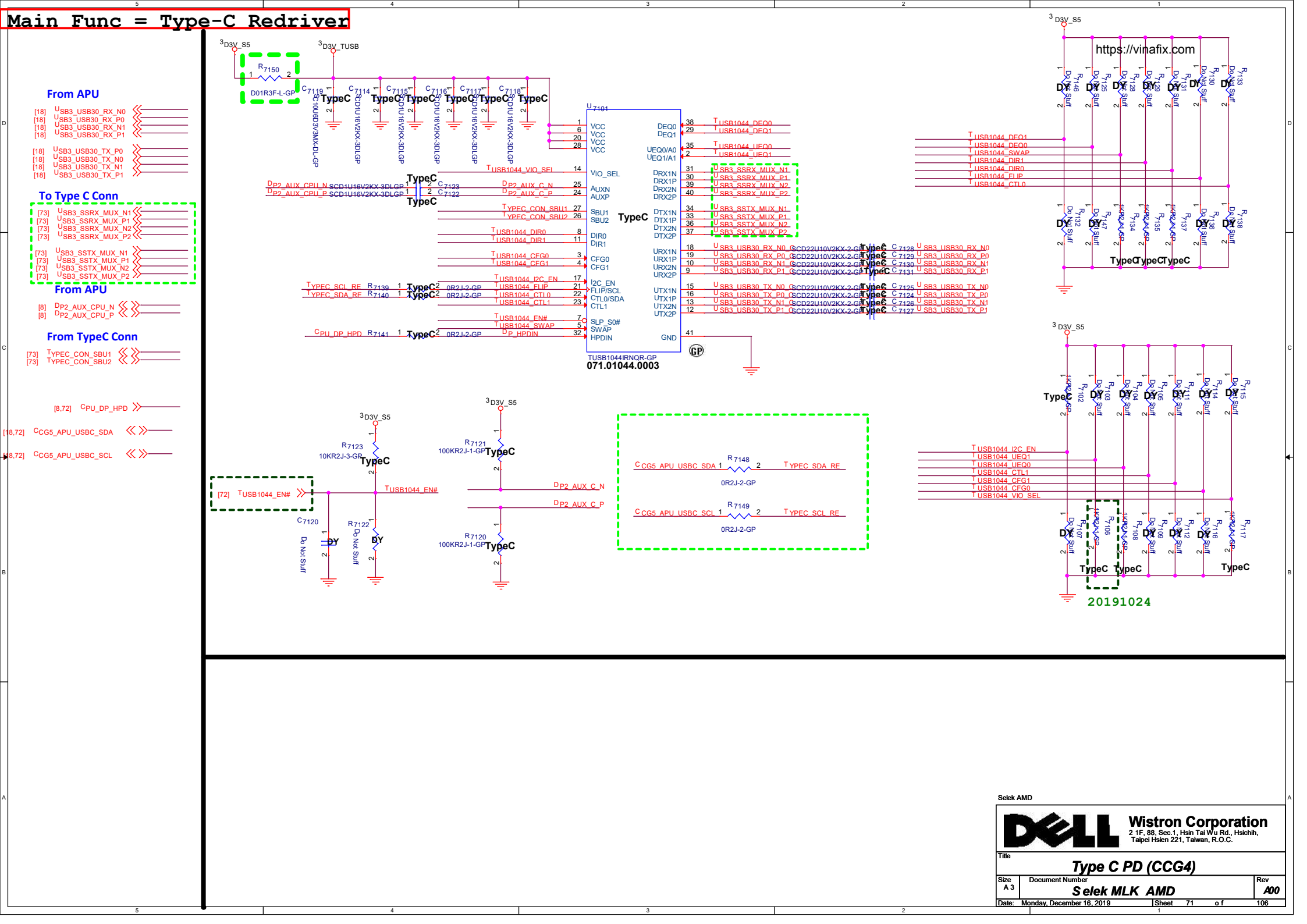
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Sensor HUB</b>			
Size A 3	Document Number		Rev
<b>Selek MLK AMD</b>		<b>A00</b>	
Date: Monday, December 16, 2019	Sheet	69	of 106

SSID = User.interface

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Title			
<b>Free Fall Sensor</b>			
Size A 3	Document Number		Rev
<b>Selek MLK AMD</b>		<b>A00</b>	
Date: Monday, December 16, 2019	Sheet	70	of 106



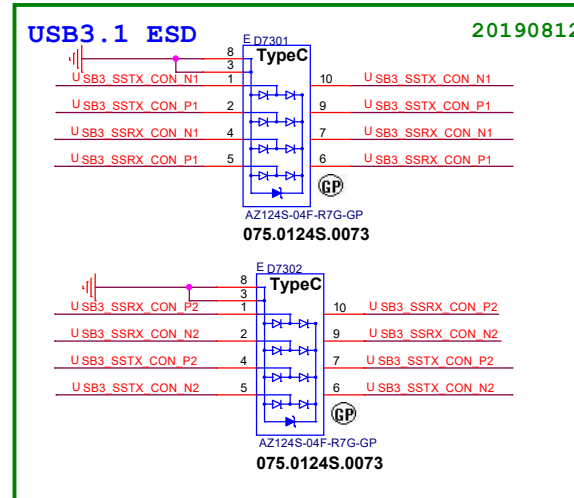
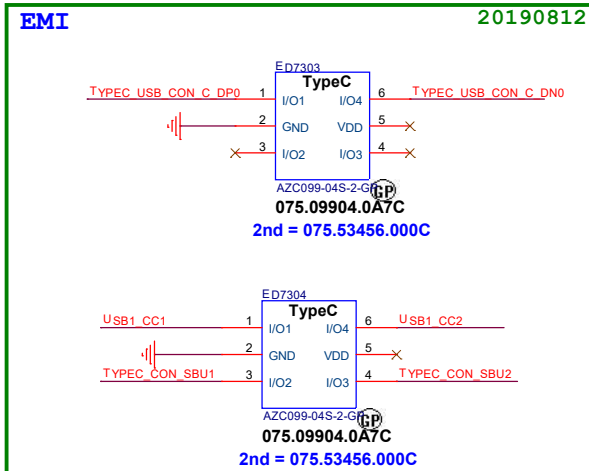
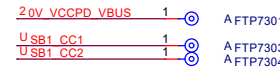
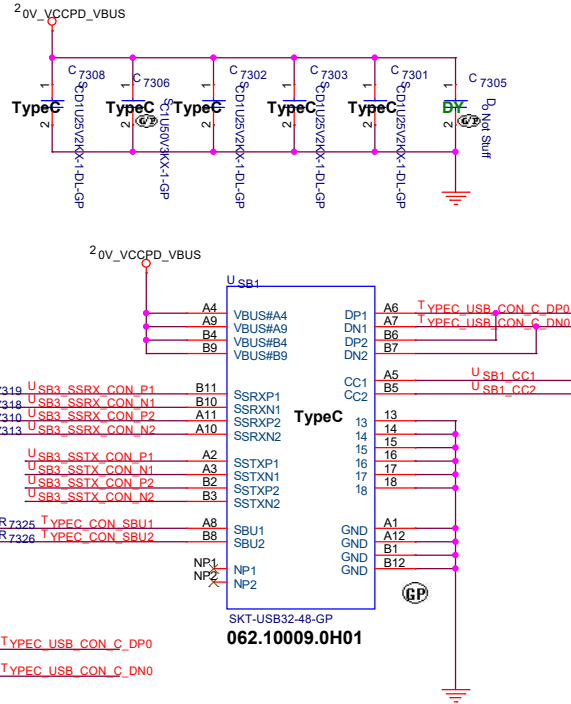
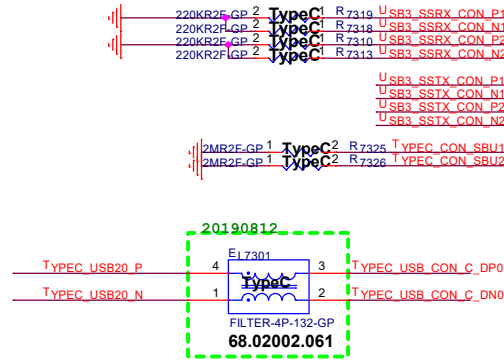
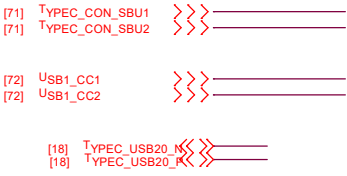


# Main Func = TYPEC CONNECTOR

## Type-C Connector

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### From Re-driver



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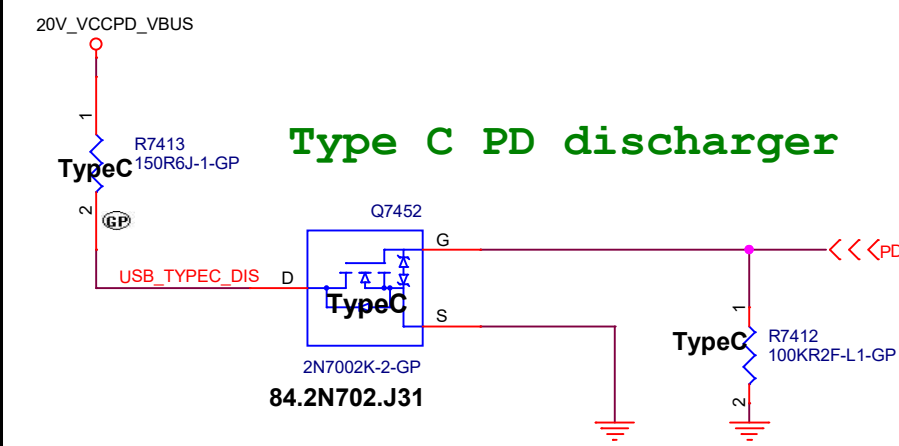
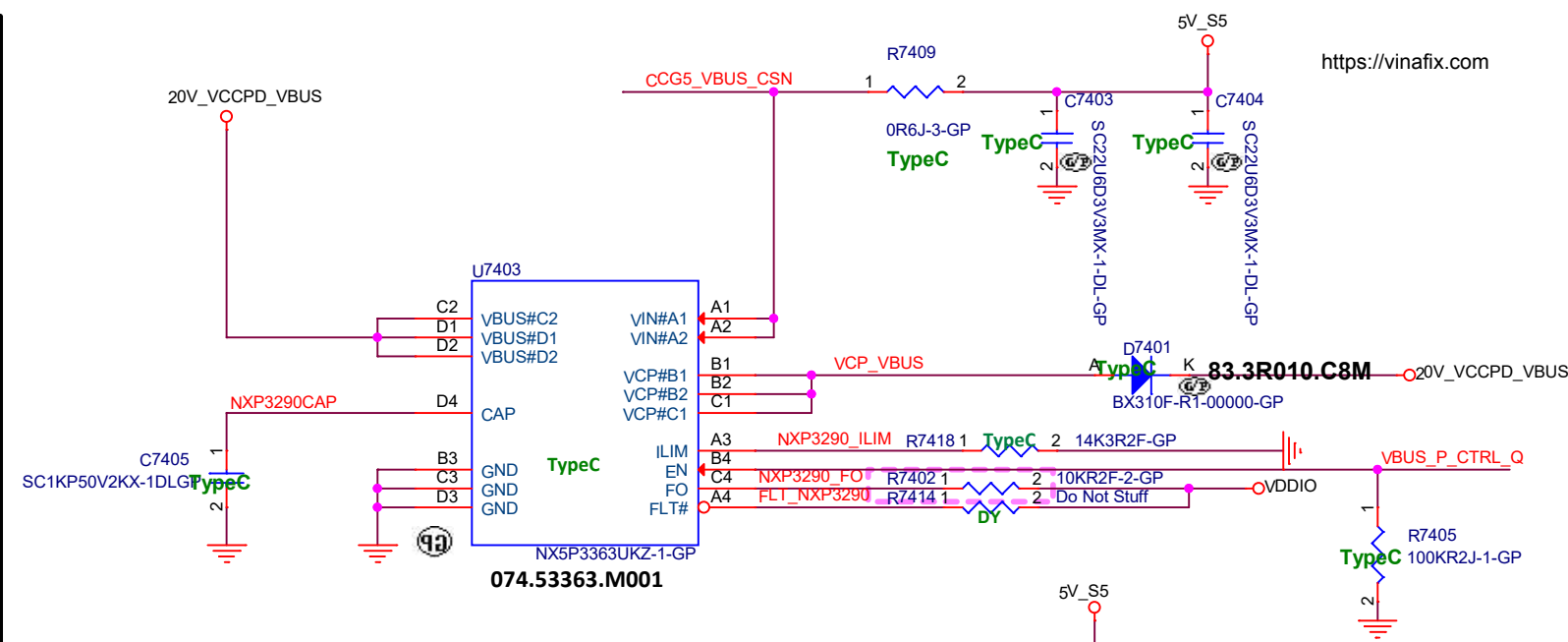
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Title			<b>TYPEC CONN</b>	
Size	Document Number	Rev		
A3		Selek MLK AMD		A00
Date:	Monday, December 16, 2019	Sheet	73	of 105

Main Func = LPS


[72] VBUS\_P\_CTRL\_Q >>>

[72] NXP3290\_FO <<<



PD\_VBUS\_DISCHG = 1 (VBUS Discharging)  
PD\_VBUS\_DISCHG = 0/Z (VBUS not discharging)

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Title: **LPS**

Size: A4	Document Number: <b>Selek MLK AMD</b>	Rev: <b>A00</b>
Date: Monday, December 16, 2019		Sheet 74 of 105

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Title			
Reserved			
Size A 3	Document Number		Rev
Selek MLK AMD		A00	
Date: Monday, December 16, 2019	Sheet	75	of 106

[16] GFX\_CLK\_CPU\_P  
[16] GFX\_CLK\_CPU\_N  
[16] REG\_CLKREQ0\_CPU\_N

[8,24] CPU\_SMB\_SCL\_EC  
[8,24] CPU\_SMB\_SDA\_EC

[3] GFX\_PCIE\_TX\_P0  
[3] GFX\_PCIE\_TX\_N0  
[3] GFX\_PCIE\_TX\_P1  
[3] GFX\_PCIE\_TX\_N1  
[3] GFX\_PCIE\_TX\_P2  
[3] GFX\_PCIE\_TX\_N2  
[3] GFX\_PCIE\_TX\_P3  
[3] GFX\_PCIE\_TX\_N3

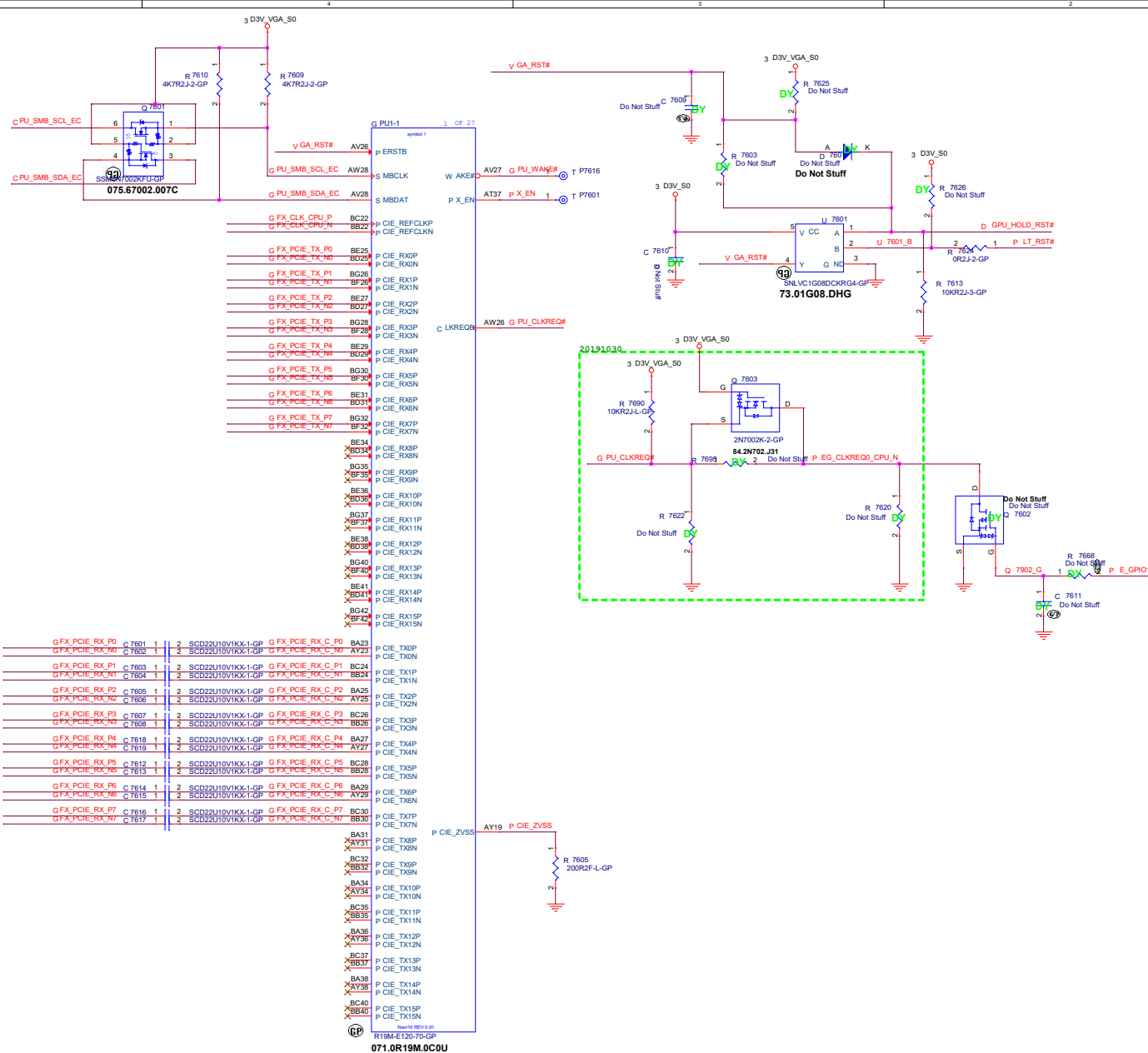
[3] GFX\_PCIE\_TX\_P4  
[3] GFX\_PCIE\_TX\_N4  
[3] GFX\_PCIE\_TX\_P5  
[3] GFX\_PCIE\_TX\_N5  
[3] GFX\_PCIE\_TX\_P6  
[3] GFX\_PCIE\_TX\_N6  
[3] GFX\_PCIE\_TX\_P7  
[3] GFX\_PCIE\_TX\_N7

[3] GFX\_PCIE\_RX\_P0  
[3] GFX\_PCIE\_RX\_N0  
[3] GFX\_PCIE\_RX\_P1  
[3] GFX\_PCIE\_RX\_N1  
[3] GFX\_PCIE\_RX\_P2  
[3] GFX\_PCIE\_RX\_N2  
[3] GFX\_PCIE\_RX\_P3  
[3] GFX\_PCIE\_RX\_N3

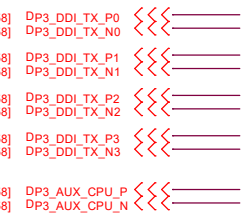
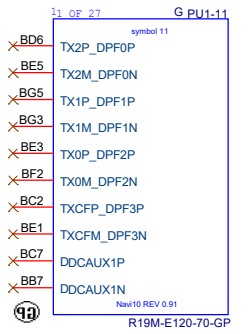
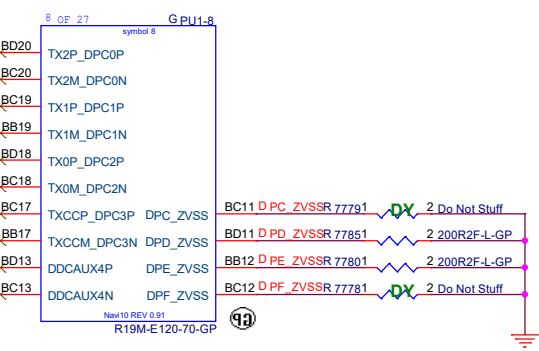
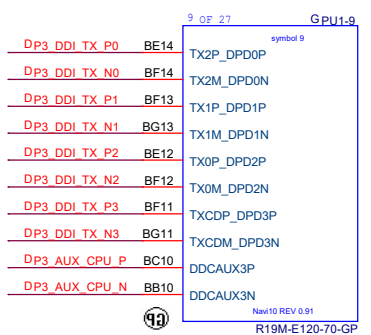
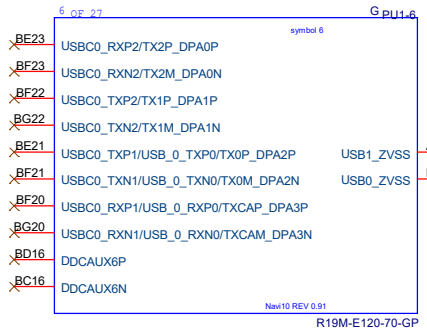
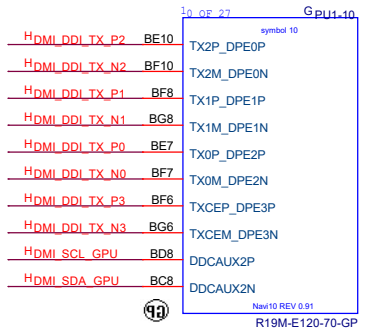
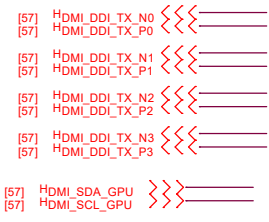
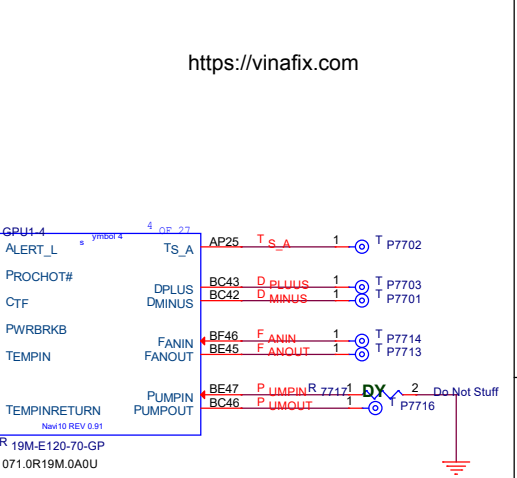
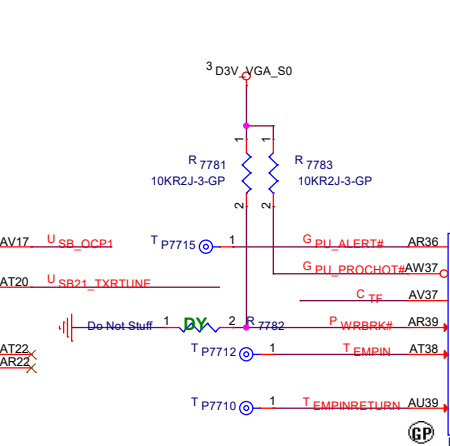
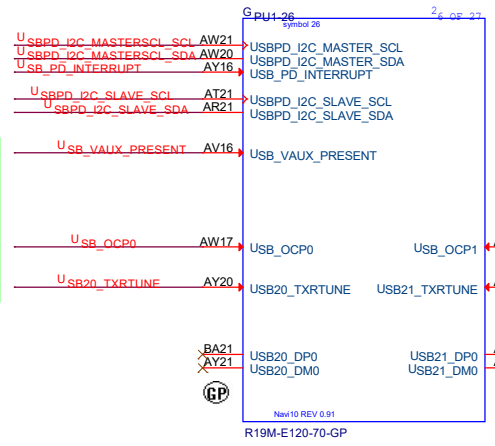
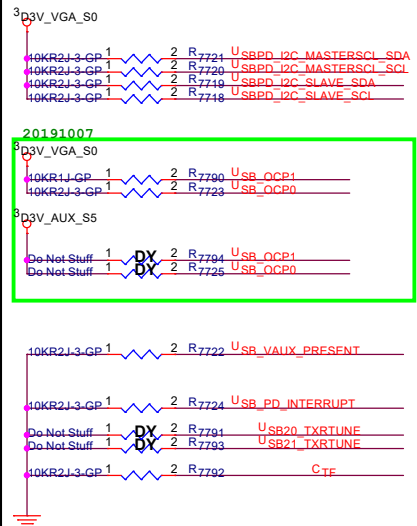
[3] GFX\_PCIE\_RX\_P4  
[3] GFX\_PCIE\_RX\_N4  
[3] GFX\_PCIE\_RX\_P5  
[3] GFX\_PCIE\_RX\_N5  
[3] GFX\_PCIE\_RX\_P6  
[3] GFX\_PCIE\_RX\_N6  
[3] GFX\_PCIE\_RX\_P7  
[3] GFX\_PCIE\_RX\_N7

[16,86] DGPU\_HOLD\_RST#  
[17,24,61,63,66,91] pLT\_RST#  
[17,86] pE\_GPD01

[87] VGA\_RST#



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Title **GPU (2/5) DIGITALOUT**

Size A 3	Document Number <b>Selek MLK_AMD</b>	Rev <b>A00</b>
Date: Monday, December 16, 2019	Sheet 77	of 106














Main Func = dGPU

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Title

GPU-VRAM7,8 (4/4)

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A 3

Document Number  
Selek MLK AMD

Rev  
A 00

Date: Monday, December 16, 2019

Sheet 84 of 106

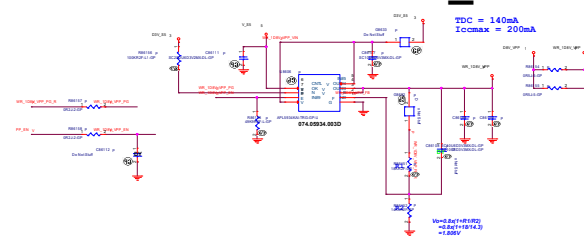
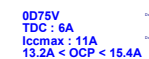


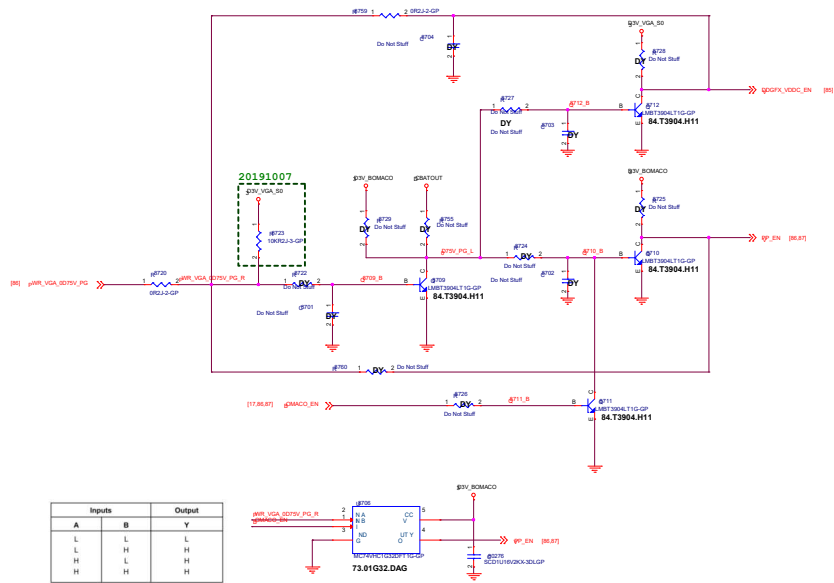


<https://vinafix.com>

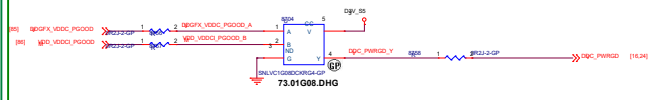


### ***APL5934 for 1D8V\_VPP***

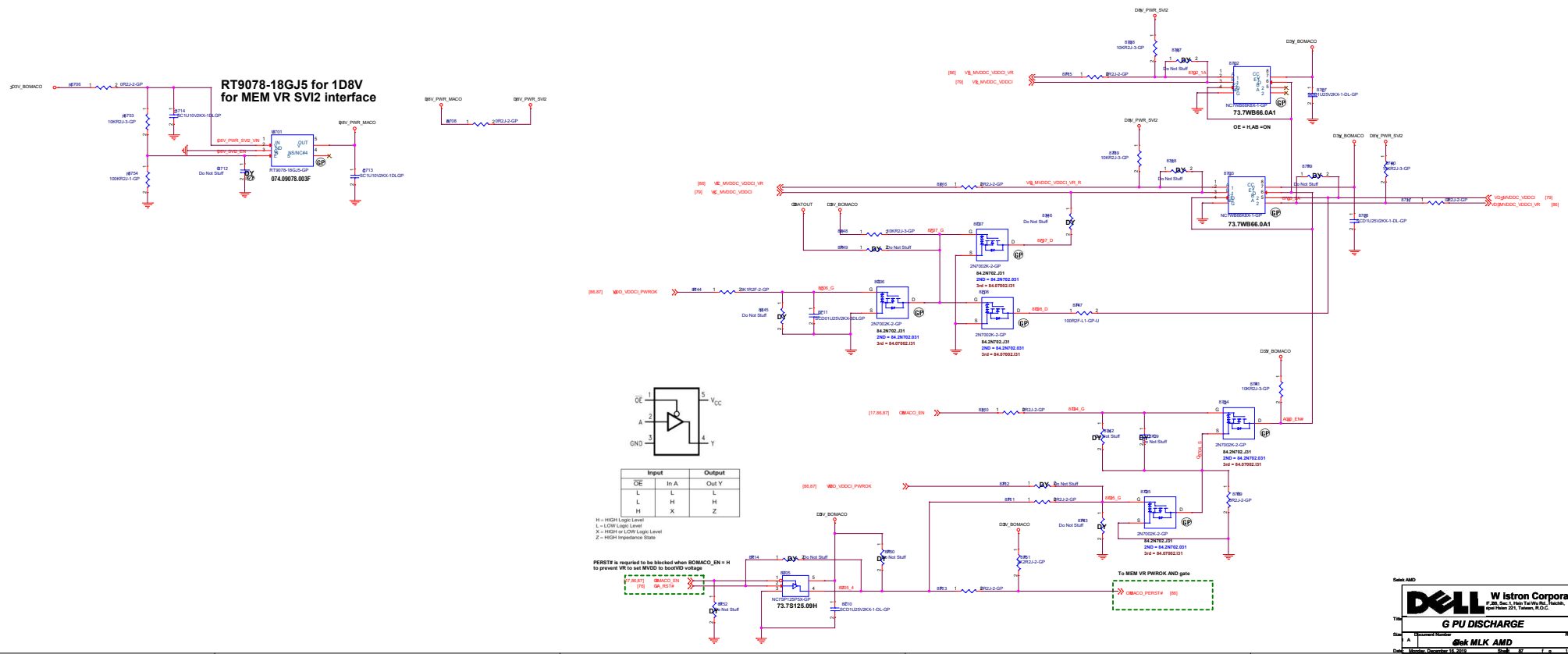
**SY8288RAC For 0D75V**



## POWERGOOD STATUS




## SVI2 BOMACO



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Title

Reserved

Size  
A 3

Document Number  
**Selek MLK AMD**

Date: Monday, December 16, 2019

Rev  
**A00**

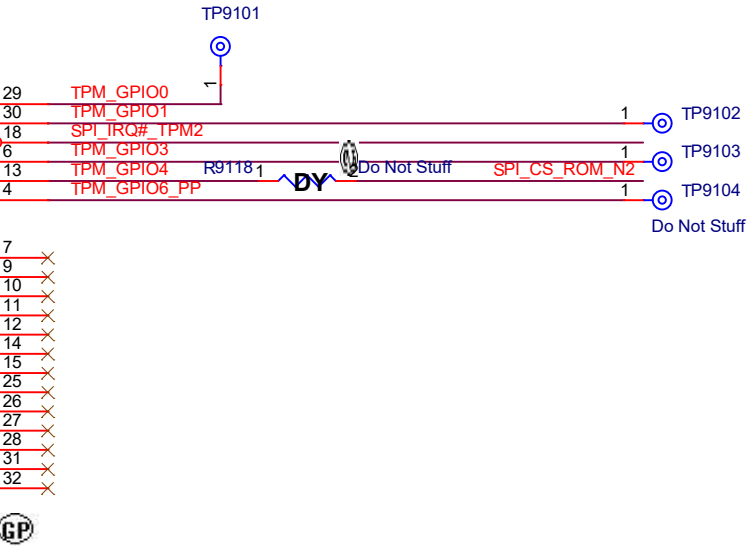
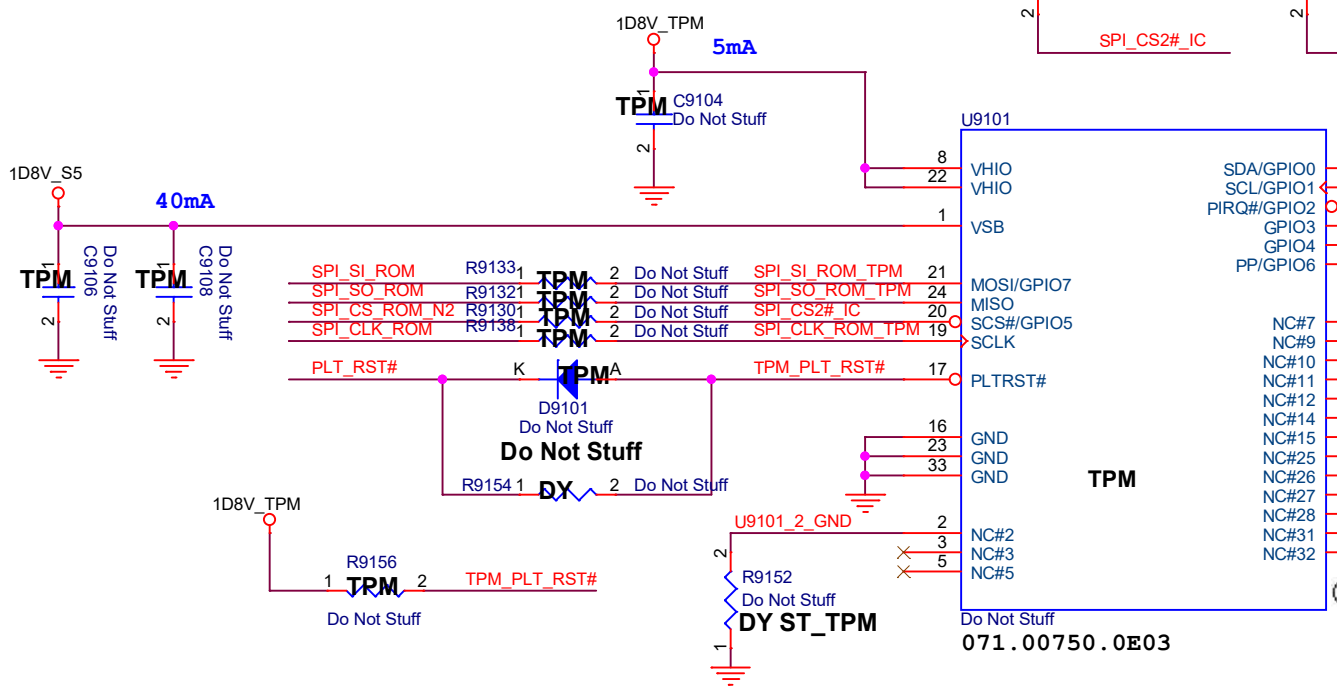
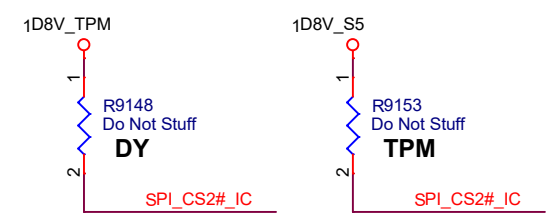
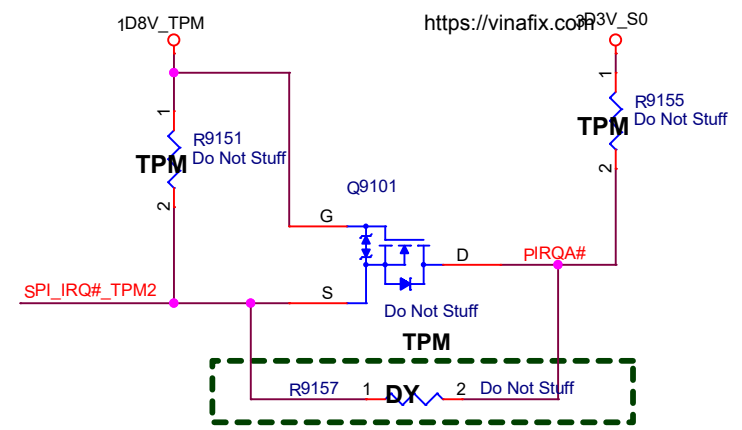
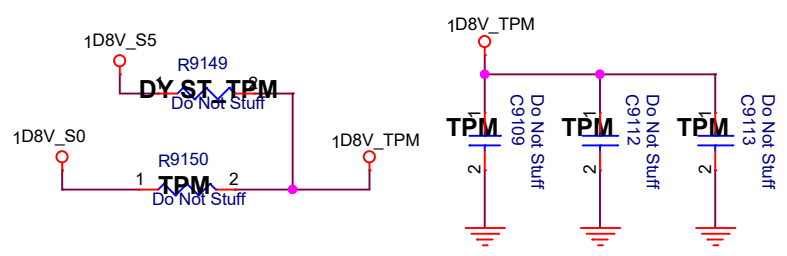
Sheet 88 of 106



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Main Func = TPM

[17,24,61,63,68,76] PLT\_RST# >>>  
[16,20,24,25] SPI\_CLK\_ROM >>>  
[16,24,25] SPI\_SI\_ROM >>>  
[16,24,25] SPI\_SO\_ROM >>>  
[16] SPI\_CS\_ROM\_N2 >>>  
[17] PIRQA# >>>



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Title **INT IO (TPM)**

Size A4	Document Number <b>Selek MLK AMD</b>	Rev <b>SB</b>
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Date: Monday, December 16, 2019 Sheet 91 of 105

# Finger Print

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[24] FPR\_SCAN# <<< —

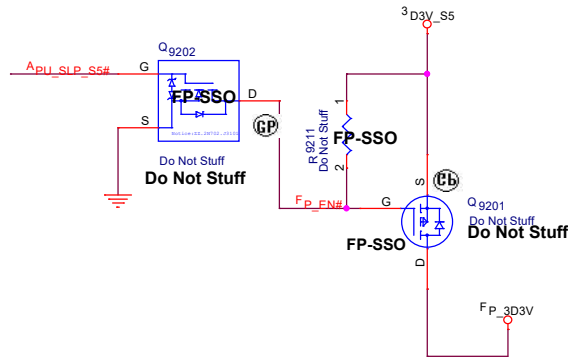
[18] FP\_USB20\_N <<< —

[18] FP\_USB20\_P <<< —

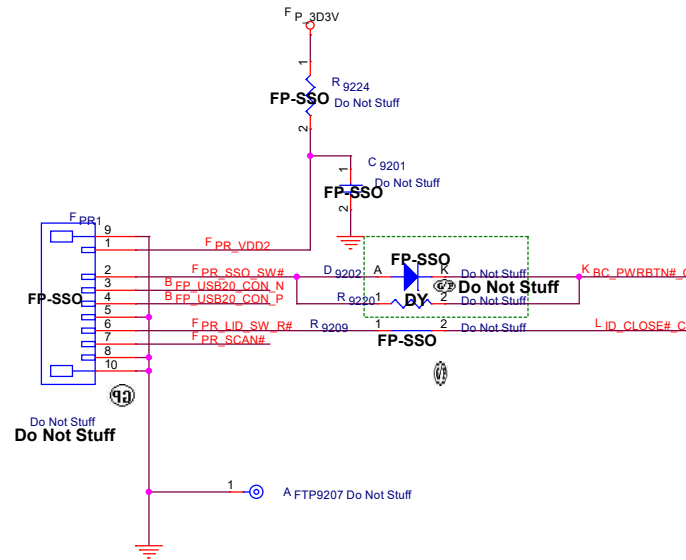
[7,24,44,51,65] APU\_SLP\_S5# >>> —

[64,66] LID\_CLOSE#\_Q >>> —

[64] KBC\_PWRBTN#\_C >>> —

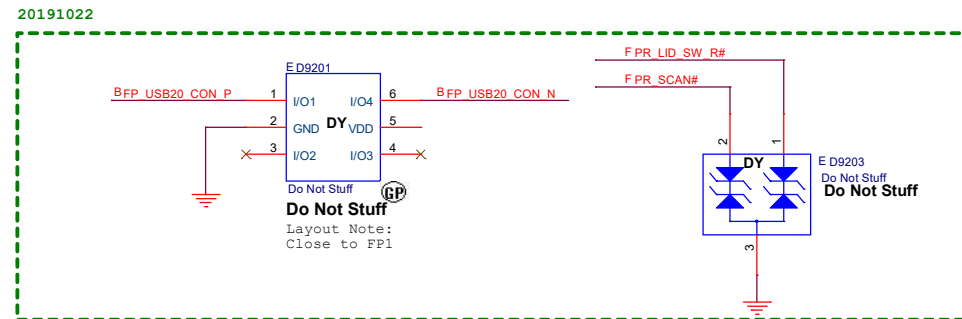
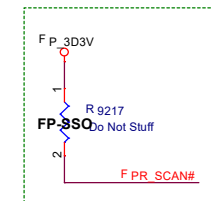
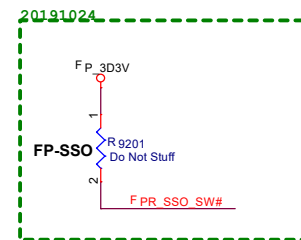
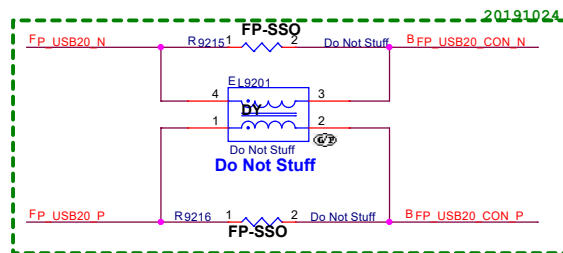


	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0



## FP Module

	Pin
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPIO_key shielding
8	GND(ID pin)



A FTP9201 1 FPR\_SSO\_SW#  
A FTP9205 1 FPR\_LID\_SW\_R#

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 Sheet 92 of 106

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Sheet 93 of 106

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Sheet 94 of 106

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Date: Monday, December 16, 2019


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Sheet 97 of 106

**LVDS\_Switch**


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<b>CRT_Switch</b>			
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**CLK Block Diagram**

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Sheet  
100 of 1

108

Change notes -

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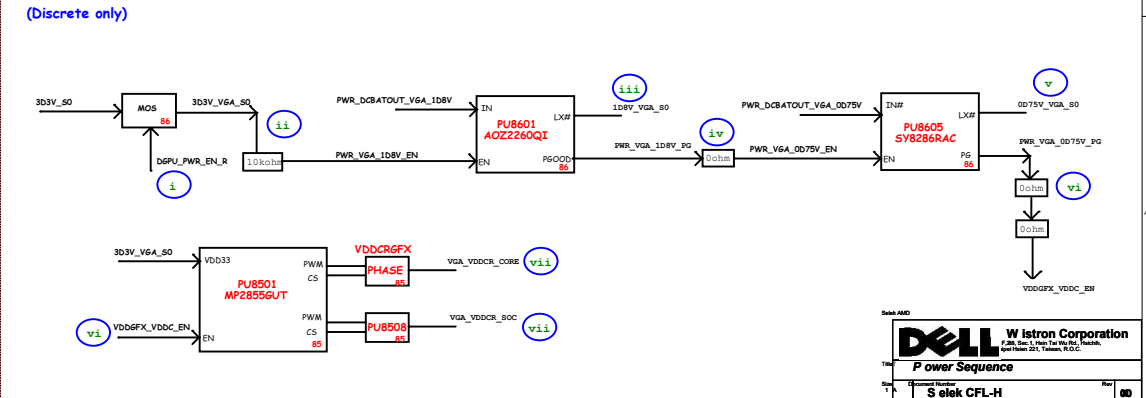
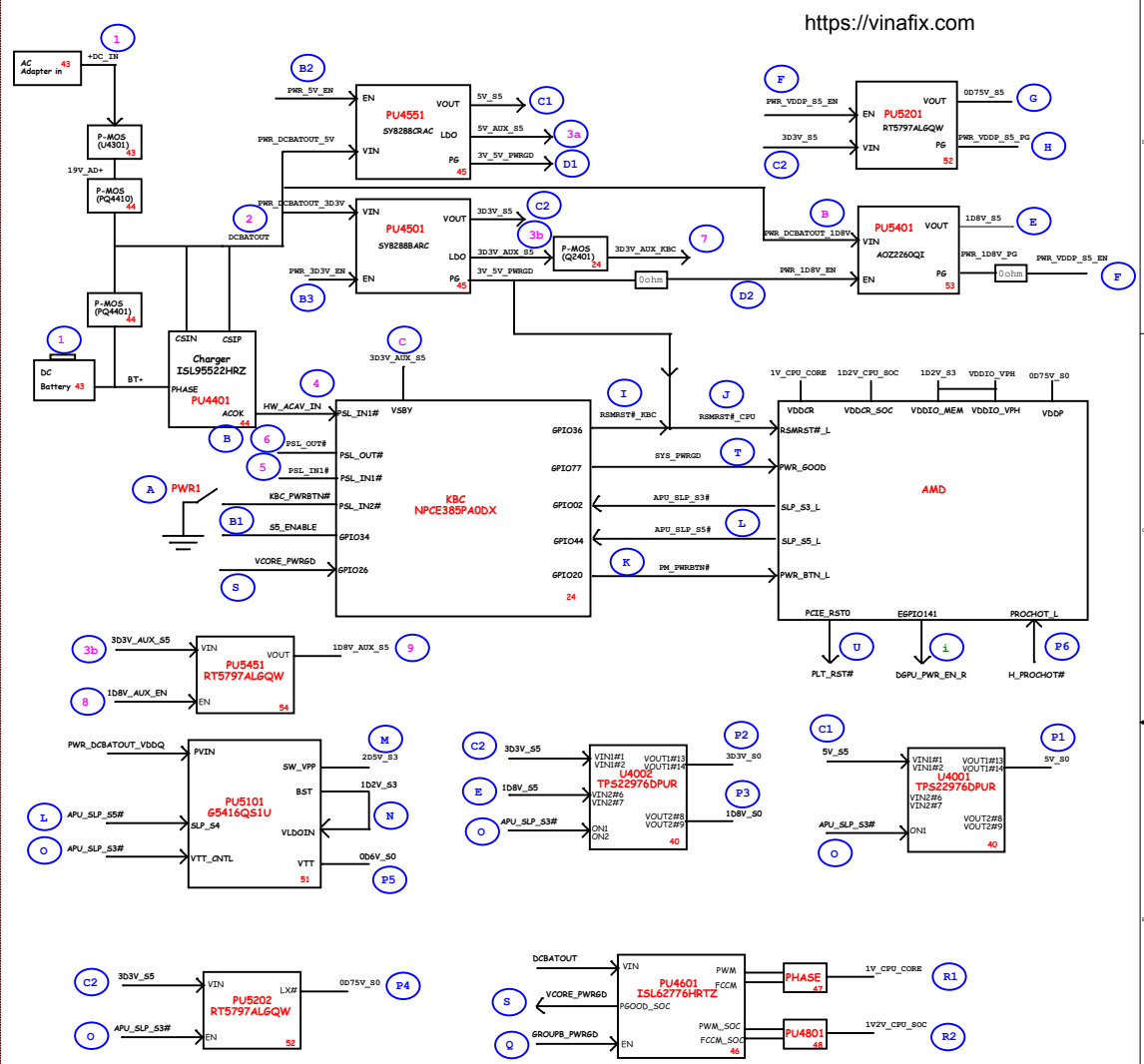
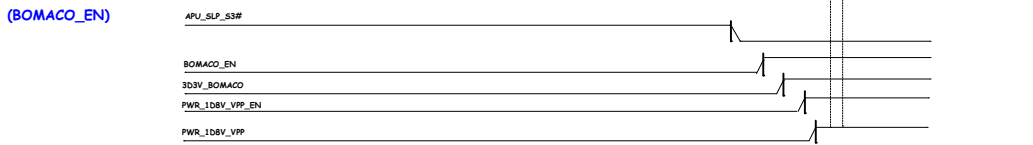
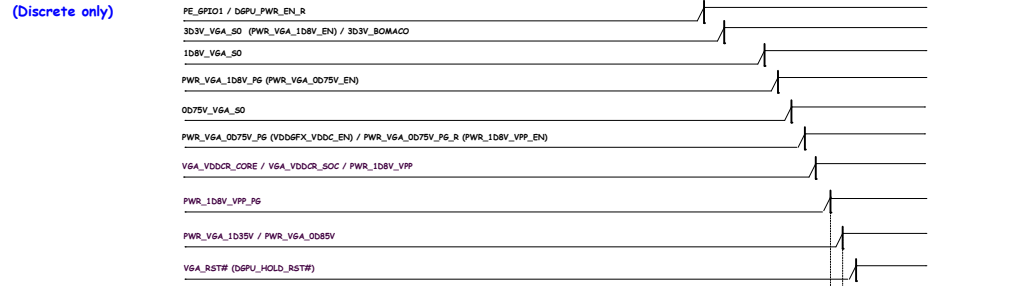
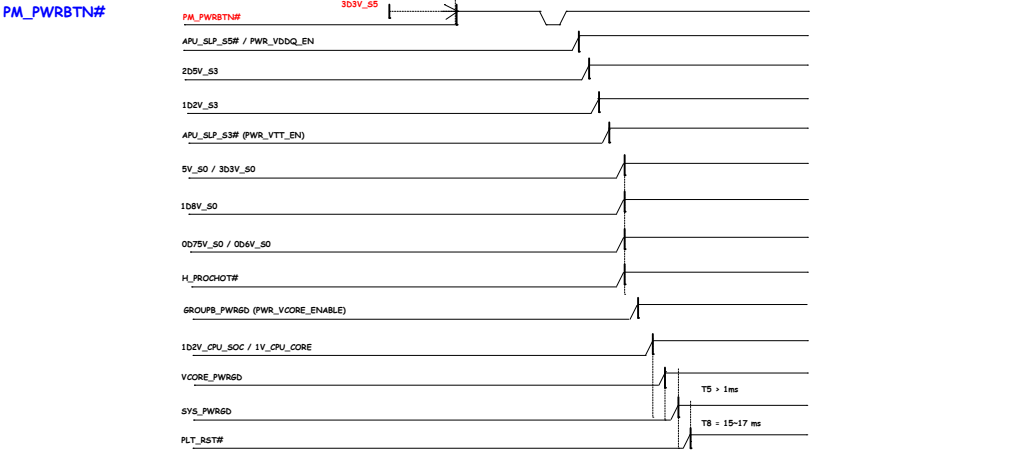
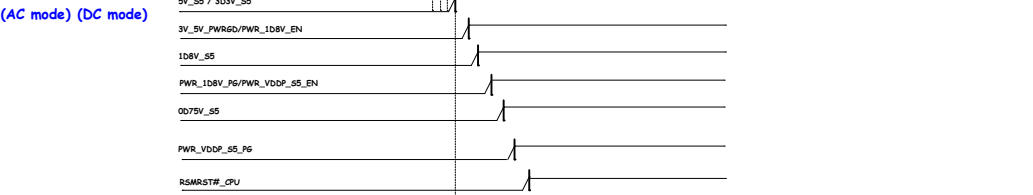
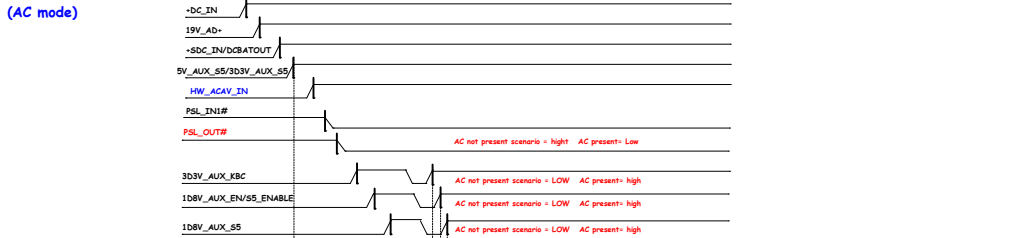
Date: Monday, December 16, 2019

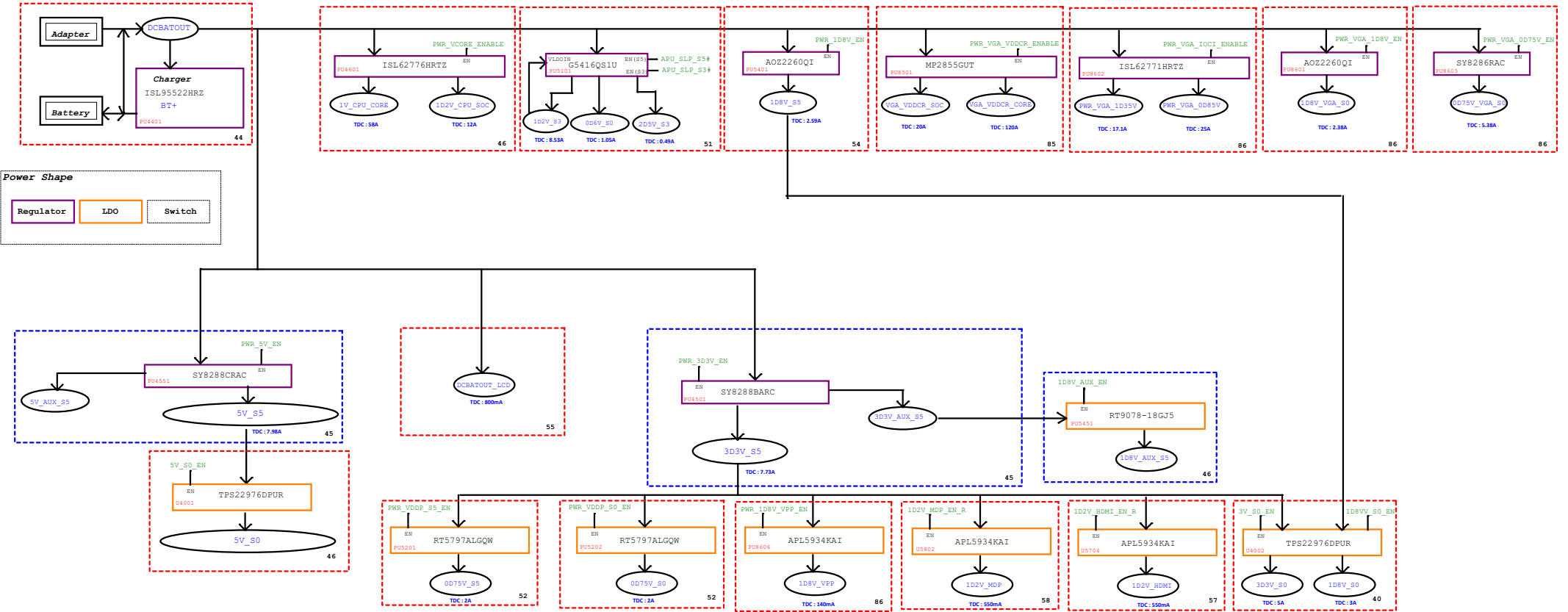
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Sheet 101 of 106


**Change History**

Power Up Sequence





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SMBUS Block Diagram

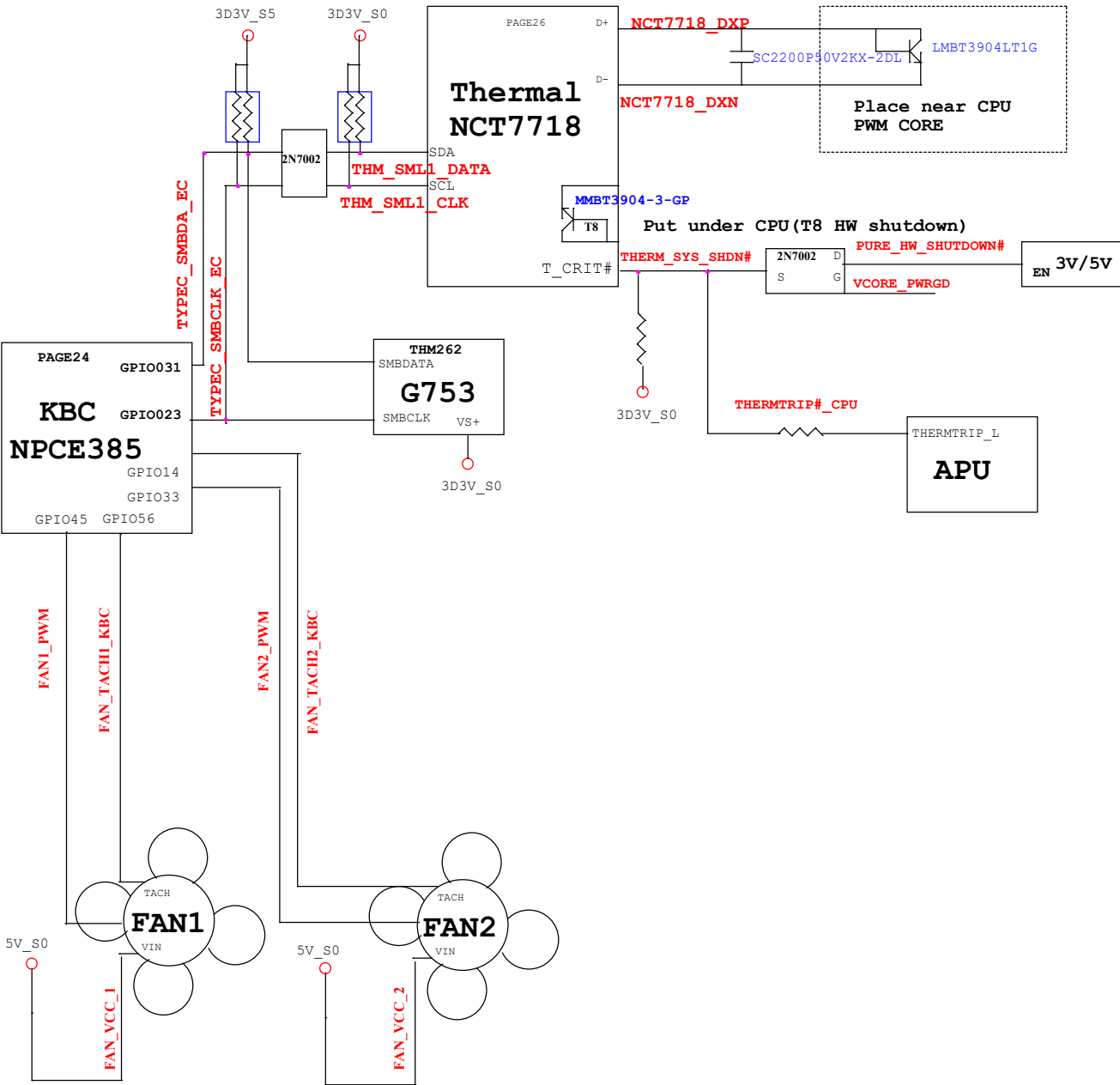
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Document Number  
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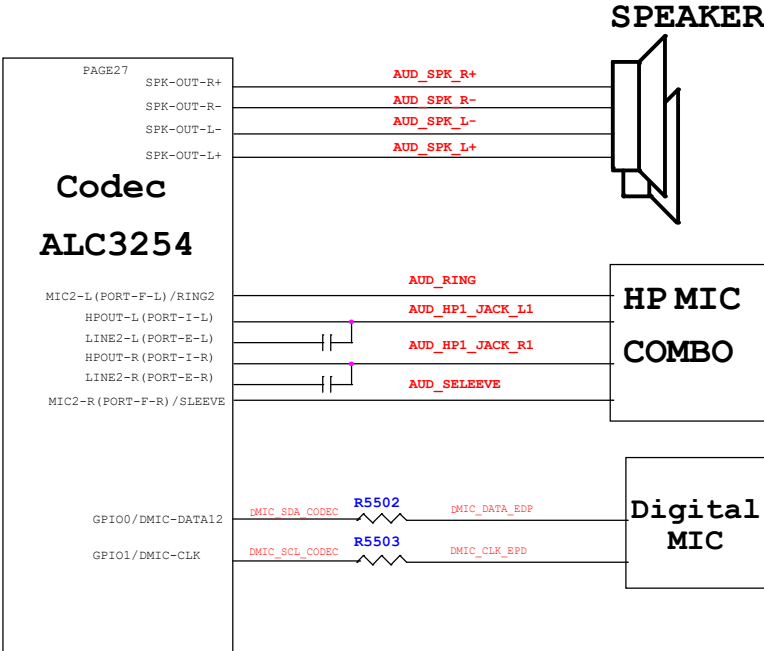
Rev  
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Date: Monday, December 18, 2018Sheet: 104 of 1108

# Thermal Block Diagram



# Audio Block Diagram



CLK Block Diagram

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